

Forward Converter with FPGA-Based Self-Tuning PID Controller

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Abstract

In this paper, based on a field programmable gate array (FPGA) technique is presented to design the PID controller and applied to the forward converter. The on-line tuning of controller parameters is used to reduce the effect of input voltage variations on the transient load response. Besides, the improvement in the transient load response is considered further, especially for the maximum input voltage. The validity of the proposed control topology is demonstrated via some experimental results.

Key Words: FPGA, Forward Converter, On-Line Tuning, PID, Transient Load Response

1. Introduction

As generally known, there are many disadvantages existing in the analogue controller, such as large system delay, noise interference, parameter variations due to thermal variations, and so on, thereby reducing the performance of the DC-DC converter. Therefore, many researches have presented digital control methods [1–16] to overcome these problems. And, among them, the microcomputer (uP) [3–5] or the digital signal processor (DSP) [6–12] has been utilized, which the switching frequency for the DC-DC converter is limited to some extent. Consequently, to overcome such this problem, a field programmable gate array (FPGA) based technique [13–16] is applied to controlling the DC-DC converter.

Unlike uP and DSP, FPGA has no problem in timing sequence, thereby allowing many processes to go at the same time with the system delay reduced as minimum as possible. This is a key point in the DC-DC converter having fast transient load response.

Recently, DC-DC converters with low output voltage and high output current have been widely used in industrial applications. Among them, the forward converter is getting more and more popular due to its inher-

ent advantages, such as isolation, stability, multi-output, etc. [17]. However, the traditional forward converter is controlled using the analogue controller and this deteriorates the performance of its transient load response. Thus, in this paper, unlike [16], in this paper a proportional-integral-derivative (PID) controller is applied to the forward converter to upgrade the accuracy of the output voltage at heavy loads. Also, in designing such a controller, the input voltage variations in the transient load response are taken into account. Moreover, to further reduce the recovery time of the transient load response, the parameter of this controller is tuned during the transient load. Herein, the detailed design procedure and some experimental results are provided to verify the effectiveness of the proposed control scheme.

2. Overall System Description

Figure 1 shows the overall system of the proposed FPGA-based PID controller for the forward converter. The main power and its peripherals containing control and protection circuits are described below.

A. Main Power Stage

The main power circuit is based on the conventional forward converter with some modifications. There is an

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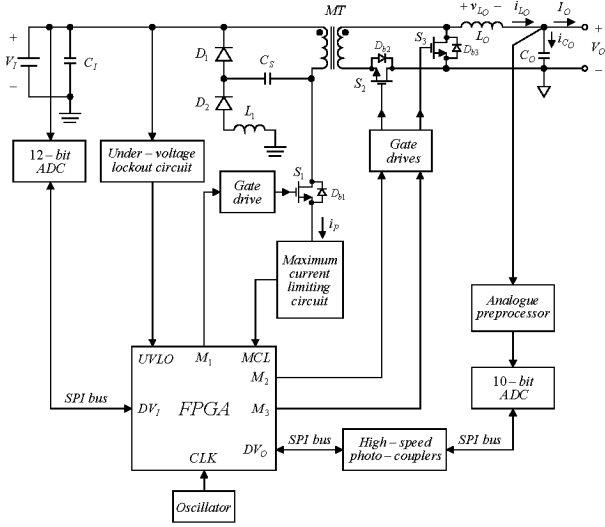


Figure 1. Overall system of the proposed FPGA-based forward converter.

inductance-capacitance LC snubber at the primary side of the main transformer MT to reset the flux as soon as the main MOSFET switch S_1 , PSMN015-100B, is turned off. Such a snubber contains the resonance capacitor C_S , the resonance inductor obtained from the magnetization inductance L_m of MT, two diodes D_1 and D_2 are utilized to reset the flux and to discharge the energy stored in the capacitor C_S through the current limiting inductor L_1 respectively. Also, there are two synchronous rectifiers, high-side MOSFET switch S_2 , PSMN015-100B, and low-side MOSFET switch S_3 , PHD96NQ03, used to replace two traditional diodes so as to enhance the efficiency of the converter. Besides, since the current supplied from FPGA is not sufficient to drive the MOSFET switches, the gate drives are added to upgrade FPGA's capability of current sourcing. The remainder of the main power stage contains the output inductor L_O and the output capacitor C_O .

1) Output inductance calculated

The inductance L_O is decided by the slew rate of the current flowing through L_O as follows, and hence

$$SR_{L_O} \triangleq \left. \frac{di_{L_O}}{dt} \right|_{t_{on}} = \frac{v_{L_O}}{L_O} \Big|_{t_{on}} = \frac{V_I / n - V_O}{L_O} \quad (1)$$

Therefore,

$$L_O = \frac{V_I / n - V_O}{SR_{L_O}} \quad (2)$$

where v_{L_O} is the voltage across L_O .

2) Output capacitance calculated

The capacitance C_O is determined by the load current slew rate from no load to rated load, SR . As shown in Figure 2, the slew rate of the ideal load current $I_{O-ideal}$ is far from larger than that of the actual load current $I_{O-actual}$. In Figure 2, ΔQ is defined as the total electric charge required to offer the load as the $I_{O-actual}$ rises from zero to 90% of variation in the load current from no load to rated load, ΔI_O , with the elapsed time Δt , and hence

$$\Delta Q = \frac{1}{2} \cdot \Delta I_O' \cdot \Delta t = \frac{1}{2} \cdot \left(\frac{9}{10} \cdot \Delta I_O \right) \frac{\left(\frac{9}{10} \cdot \Delta I_O \right)}{SR} = \frac{81 \cdot \Delta I_O^2}{200 \cdot SR} \quad (3)$$

Also,

$$\Delta Q \cong C_O \cdot \Delta V_{CO} \quad (4)$$

Therefore,

$$C_O \cong \frac{81 \cdot \Delta I_O^2}{200 \cdot SR \cdot \Delta V_{CO}} \quad (5)$$

where ΔV_{CO} denotes the peak-to-peak voltage created from C_O due to ΔI_O .

B. Under-Voltage Lockout Circuit

The under-voltage lockout (UVLO) circuit is utilized to start this converter under the condition that the input voltage goes up to some one value, as well as to make this converter fail in operation if the input voltage falls down to some other value, so as to avoid undesired destruction of the component and error action of the system.

C. Maximum Current Limiting Circuit

The maximum current limiting (MCL) circuit is used

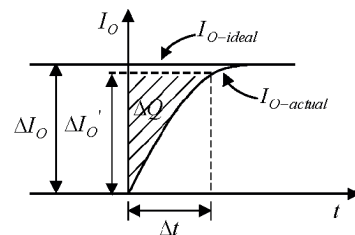


Figure 2. Slew rate of the load current.

to protect the converter from being damaged during an over-current fault condition. It also enables the converter to restart when the fault is removed.

D. High-Speed Photo-Couplers

High-speed photo-couplers, HCPL2631 with two in one, are used not only to isolate FPGA from the secondary side of MT but also to transfer the signal to FPGA as fast as possible.

E. Analogue Preprocessor and ADCs

The analogue preprocessor is employed to get information on the actual output voltage before one 10-bit analogue-to-digital converter (ADC), TLV1572, operates, whereas the other 12-bit ADC, ADCS7476, is used to get information on the actual input voltage. Also, the series peripheral interface (SPI) is utilized to communicate between FPGA and ADCs. It is noted that the actual output voltage is sampled in the middle of the turn-on interval to avoid noise interference.

F. Oscillator and FPGA

The oscillator is utilized to provide the clock, CLK, to FPGA, EP1PC3. The purpose of FPGA is to execute logic operation. Then, the resultant digital signals, created from the UVLO circuit, the MCL circuit, and the ADCs for the input and output voltages, are all sent to FPGA to involve generating the required PWM signals.

3. Design Considerations

The design specifications of the proposed forward converter are given as follows.

Rated input DC voltage: $V_I = 12\text{V}$

Input DC voltage range: $V_I = 12$ to 18V

Turn ratio of the main transformer: $n = n_p/n_s = 6/5$

Output DC voltage: $V_O = 5.12\text{V}$

Rated output DC current: $I_{O-rated} = 10\text{A}$

Current slew rate of L_O : $SR_{L_O} = 2\text{A}/\mu\text{s}$

Output current slew rate from no load to rated load: $SR = 10\text{A}/\mu\text{s}$

Switching frequency at rated load: $f_s = 195\text{ kHz}$ ($100\text{ MHz} \div 512$)

Maximum output voltage ripple: $\Delta V_{O_max} = 100\text{ mV}$

Operating condition at rated load: Continuous conduction mode (CCM)

A. Main Power Stage

Since the procedure for the overall circuit design begins from the point of view of the current slew rate of the output inductor, the output inductor can be calculated to be $2.5\text{ }\mu\text{H}$ based on (2). Therefore, an inductor, HK-RM136-15A1R4, is chosen herein, whose value is about $2.2\text{ }\mu\text{H}$ at rated load. Moreover, the duty cycle is obtained to be 0.5 from calculation under these conditions. Consequently, the peak-to-peak current flowing through the output inductor is calculated to be about 5A that is smaller than the rated output current, meaning that this converter operates from the discontinuous conduction mode (DCM) to the continuous conduction mode (CCM) if the load is altered from no load to rated load.

Regarding the output capacitance C_O , it is determined according to (5) and under the assumption that $\Delta V_{CO} \leq 10\text{ mV}$, and hence C_O is larger than $405\text{ }\mu\text{F}$. Accordingly, two solid tantalum chip capacitors, T510X477006As, connected in parallel, are chosen for C_O , whose value is reduced to about $500\text{ }\mu\text{F}$ at the switching frequency of 195 kHz , and the corresponding equivalent series resistance (ESR) is about $15\text{ m}\Omega$, a typical value from the associated datasheet. Based on the mention above, the maximum output voltage ripple is about 90 mV , within the design specifications.

As for the LC resonance snubber, the resonance inductance is the magnetization inductance of MT and is measured to be $110\text{ }\mu\text{H}$. Also, if the maximum voltage across the resonance capacitor C_S is set to two times the input DC voltage, then based on [16], the value of C_S , varied with frequency greatly, is obtained to be 4.4 nF . Therefore, the resonance period is about $4.4\text{ }\mu\text{s}$, the one forth times which is a critical value used to determine the resetting time of MT.

B. Protection Function

There are two protection functions used in this converter. One is the under-voltage lockout (UVLO) function, which activates the system if the input voltage runs above 11V and shutdowns the system if the input voltage falls below 10.4V . Another is the maximum current limiting (MCL) function that forces the pulse width modulation (PWM) signal to be at the voltage reference low when i_P shown in Figure 1 is over 15A but makes the system normally work as soon as this fault is removed.

C. Oscillator and FPGA

As displayed in Figures 1 and 3, the external clock, CLK, created by the oscillator, is set to 20 MHz, which is used as the system clock of FPGA. The functions created by FPGA are phase lock loop, PID controller, DPWM ROM, input voltage ADC interface, output voltage ADC interface, and main processor. Phase lock loop is used to generate 40 MHz to control the conversion time of ADC and 100 MHz for the system clock; PID controller, characteristic of on-line tuning, is to control output voltage behavior; DPWM ROM is a lookup table through which the required turn-on period of the PWM signal to control the MOSFET switch is generated via the PID controller. Regarding the input and output voltage interfaces, they are used to get input and output voltage data for the main processor via the communications protocol of SPI which is utilized to communicate between FPGA and ADCs. As for the main processor, it is the control kernel, not only to control sample enabling, but also to collect all data created from the functions mentioned above to yield suitable gate-driving signals.

D. PID Controller with Parameters On-Line Tuned

In this paper, the proportional plus integral and differential (PID) controller, shown in Figure 4, is used herein and applied to controlling the output voltage of the forward converter. The behavior of such a controller

is described as follows. Since the power supply, having positive output voltage only, feeds the components on the secondary, the analogue preprocessor is needed to do something before the 10-bit ADC. That is to say, the sensed output voltage information is sent to the 10-bit ADC that has 4 mV per LSB, via the analogue processor which is used to subtract the sensed output voltage from the reference voltage, 4.096V, and afterwards the corresponding error is doubled. The value of the output of this ADC is subtracted from the digital reference, 512, to obtain the value of the control error, e_{con} , which, together with the input voltage, v_i , involves creating the control force, f_{con} , through the on-line tuned PID controller. For example, if the sensed output voltage is 4.096V, then e_{con} is 512; if the sensed output voltage is 5.12V, then e_{con} is 0; if the sensed output voltage is 6.144V, then e_{con} is -512. The result outputted from such a controller is sent to 9-bit duty cycle generator with a DPWM gain equal to 1/512, so as to create an appropriate duty cycle to drive the plant $P(z)$ to get the desired output voltage. It is noted that as generally recognized, variations in the input voltage significantly effect on the output voltage. The higher the input voltage, the more the oscillation tends to occur, if the system is designed based on the lowest input voltage. Therefore, on-line tuning of the parameter of the designed controller is proposed, along with accelerating the transient load responses considered.

- 1) Step 1: The proportional gain k_p is tuned from zero to the value which makes the output voltage close to about 75% to 85% of the preset output voltage. And finally, k_p is chosen to be 6.
- 2) Step 2: After this, the integral gain k_i is tuned based on measurements from the oscilloscope. Therefore, during the period of the transient load response, if k_i is large enough to make the output voltage oscillate, then k_i will be reduced to some value without oscillation. And finally, k_i is obtained to be 0.5.
- 3) Step 3: From this time onward, the differential gain k_d which is selected to be 4 is added to improve the tran-

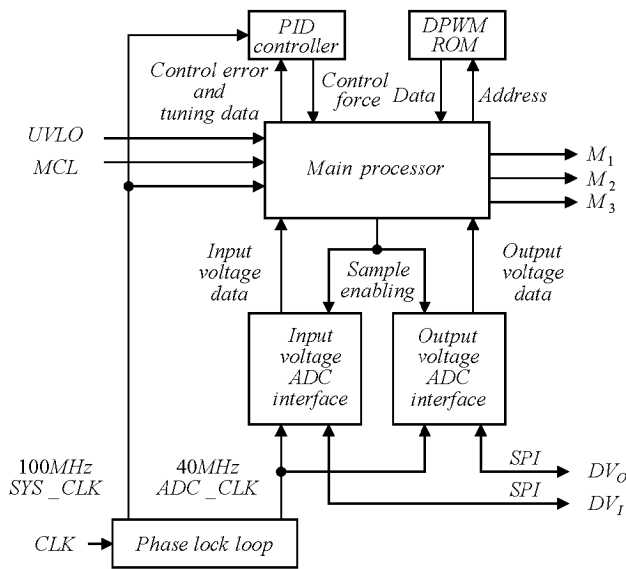


Figure 3. Functions created by FPGA.

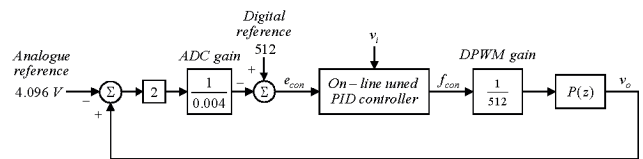


Figure 4. Control block diagram.

- 4) Step 4: Change the input DC voltage to the value of 15V, and find the transient load response has oscillation. So, k_p is reduced to 5 to eliminate oscillation in this case. Also, the transient load response of the input DC voltage of 18V is also checked and hence k_p is set to 4 in this case.
- 5) Step 5: Check the transient load response for the overall range of the desired input DC voltage with the corresponding value of k_p .
- 6) Step 6: To further enhance the transient load response, k_p is varied during the transient. If the output voltage, depicted in Figure 5, is dropped to 4.992V or less, then k_p is added by one, whereas if the output voltage is rising to 4.992V or more, then the value of k_p is recovered to the original value.

To demonstrate the validity of the proposed FPGA-based controller applied to the forward converter depicted in Figure 1, some experimental results are provided based on the mention in Sec. III.4. Figure 6 depicts the measured transient load response due to the load change from rated load to no load, at the rated input DC voltage of 12V. And Figure 7 describes the measured transient load response due to the load change from no load to rated load with the load current slew rate set to 10A/ μ s, at the rated input DC voltage of 12V. On the one hand, Figure 8 displays the measured transient load response under the same conditions shown in Figure 6 except that the input DC voltage is changed to 15V, the resulting oscillation occurs. However, under the same conditions described in Figure 6, with on-line tuning applied

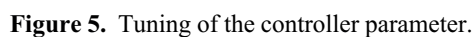


Figure 8. At the input voltage of 15V, without on-line tuning, the output voltage v_O under the load current I_O changed from rated load to no load.

controller, Figure 11 shows the measured transient load response has no oscillation. Furthermore, under the same conditions described in Figure 11, with an acceleration strategy applied to the controller, Figure 12 shows the resulting recovery time is shortened to about 30 μs .

Further to demonstrate the proposed control strategy, the input voltage is changed to 18V. On the one hand, Figure 13 displays the measured transient load re-

sponse under the same conditions shown in Figure 6 except that the input DC voltage is changed to 18V, the resulting oscillation occurs. However, under the same conditions described in Figure 6, with on-line tuning applied to the controller, Figure 14 shows the measured transient load response has no oscillation. On the other hand, Figure 15 displays the measured transient load response under the same conditions shown in Figure 7 except that the

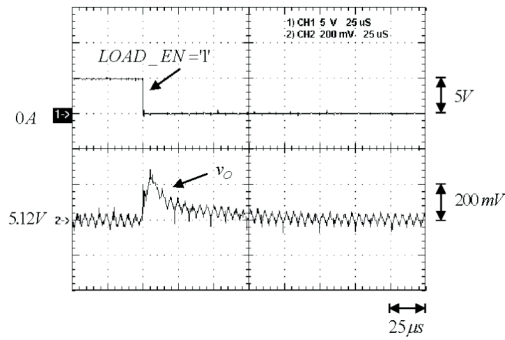


Figure 9. At the input voltage of 15V, with on-line tuning, the output voltage v_O under the load current I_O changed from rated load to no load.

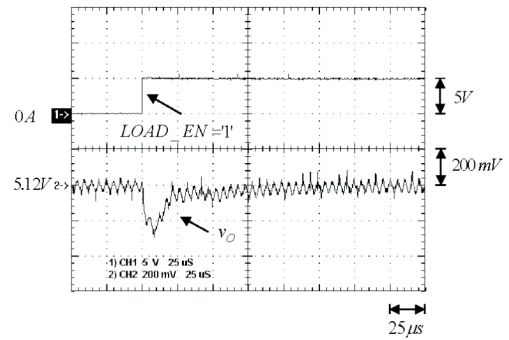


Figure 12. At the input voltage of 15V, with on-line tuning and acceleration, the output voltage v_O under the load current I_O changed from no load to rated load.

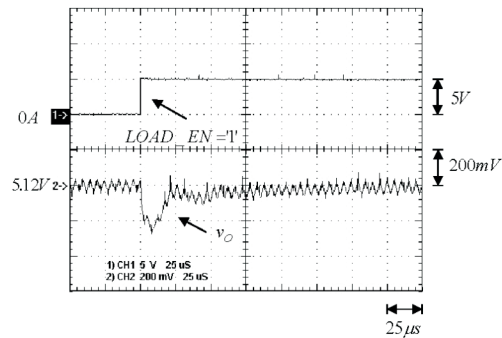


Figure 10. At the input voltage of 15V, without on-line tuning, the output voltage v_O under the load current I_O changed from no load to rated load.

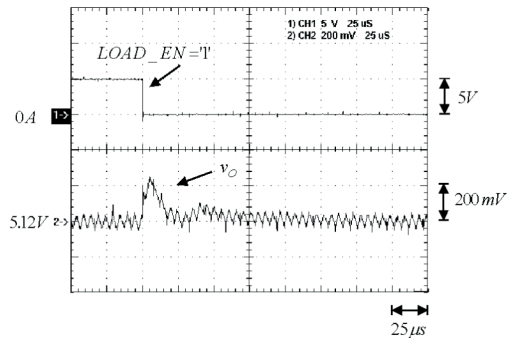


Figure 13. At the input voltage of 18V, without on-line tuning, the output voltage v_O under the load current I_O changed from rated load to no load.

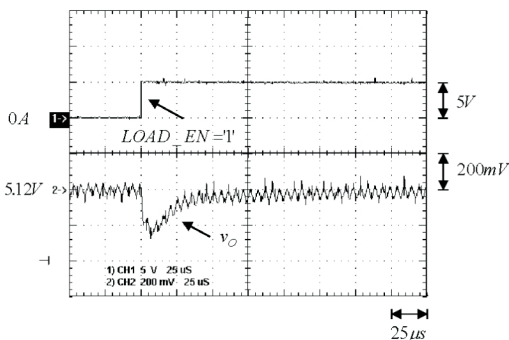


Figure 11. At the input voltage of 15V, with on-line tuning, the output voltage v_O under the load current I_O changed from no load to rated load.

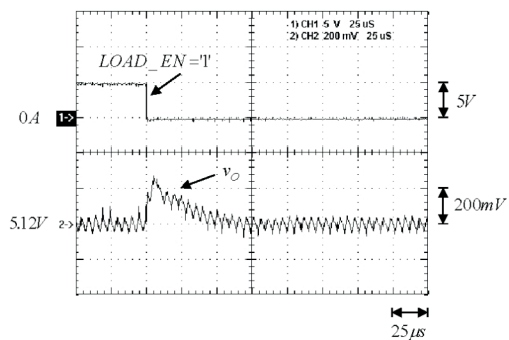


Figure 14. At the input voltage of 18V, with on-line tuning, the output voltage v_O under the load current I_O changed from rated load to no load.

input DC voltage is changed to 18V, the resulting oscillation occurs. However, under the same conditions described in Figure 6, with on-line tuning applied to the controller, Figure 16 shows the measured transient load response has no oscillation. Furthermore, under the same conditions described in Figure 16, with an acceleration strategy applied to the controller, Figure 17 shows the resulting recovery time is shortened to about 40 μ s.

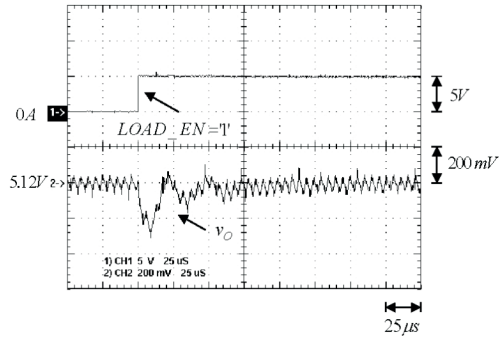


Figure 15. At the input voltage of 18V, without on-line tuning, the output voltage v_O under the load current I_O changed from no load to rated load.

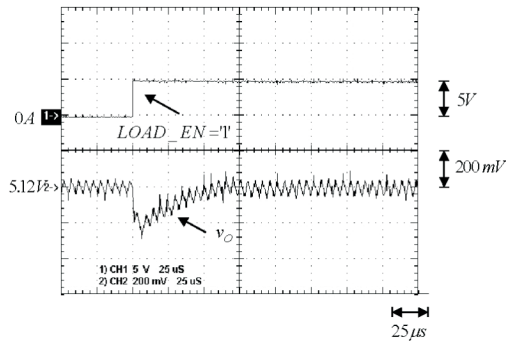


Figure 16. At the input voltage of 18V, with on-line tuning, the output voltage v_O under the load current I_O changed from no load to rated load.

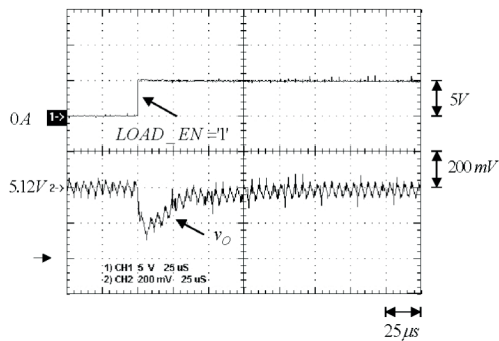


Figure 17. At the input voltage of 18V, with on-line tuning and acceleration, the output voltage v_O under the load current I_O changed from no load to rated load.

According to the experimental results mentioned above, the performance of the forward converter based on the proposed control strategy is significantly improved.

5. Conclusion

In this paper, the digital control based on FPGA is applied to the forward converter to upgrade the performance of the transient load response due to variations in input DC voltage, by adjusting the proportional gain of the PID controller. Such a control topology is applied not only to the forward converter but also to any isolated or non-isolated converter or any inverter.

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