A New High Gain AC-Decoupled Transformerless Inverter for Photovoltaic Applications

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Transformerless inverters are prominently used in the single-phase grid-connected system due to their reduced size, weight, and high efficiency. Common-mode leakage current is the main issue of transformerless inverters, which has to be mitigated. An AC-decoupled high gain inverter is proposed in the inverter capable of attaining the gain more than ten times. Hence, even if the PV voltage is less, the inverter can continue to supply the grid. Unlike the two-stage inverters, the proposed inverter doesn't require the DC-link capacitor, and it's charging diode between the boosting and inverter stages. The AC-decoupling method used in the inverter helps to reduce the leakage current within the German standard limit VDE0126-1-1. A detailed steady-state analysis of the inverter is presented. The proposed inverter is simulated in the MATLAB Simulink platform to validate its working principle. The comparative loss and thermal analysis of the semiconductor switches made of three different materials (Gallium Nitride, Silicon Carbide, and Silicon) are made in the PLECS platform. The comparative analysis proves that the proposed inverter with Gallium Nitride made switches offers higher efficiency and reliability.

Keywords: Transformerless inverter, Common-mode voltage, Common-mode leakage current, Loss analysis.

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1. Introduction

In recent years the PV-integrated grid-connected systems have been extensively advanced [1]. A small high-frequency transformer on the DC side or a bulky low-frequency transformer on the AC side provides galvanic isolation [2]. This transformer increases the size, cost, and losses. The transformerless inverter (TLI) can improve the efficiency by 1-2%. However, common-mode leakage current (CMLC) is the major issue, which has to be mitigated in TLI [3]. The PV panel ground capacitance makes the path for CMLC. The CMLC increases the grid current distortion and losses. CMLC affects the ground fault protection system and generates electroshock (Fig. 1(a))[4]. Fig. 1(b),(c) and (d) show the configuration and common-mode model of TLI. The total common-mode mode voltage (V_{TCM}) is derived from the Fig. 1(b) and given in Eq. (1). The Common mode leakage current (iCM) is derived from the Fig. 1(d) and given in Eq. (2).

$$V_{TCM} = V_{CM} + \frac{V_{DM}\,(L_{f2} - L_{f1})}{2\,(L_{f2} + L_{f1})} \tag{1}$$

where, $V_{CM} = \frac{V_{AN}+V_{BN}}{2}$; $V_{DM} = (V_{AN} - V_{BN})$. The terms VCM and VDM represent the common-mode voltage and differential-mode voltage, respectively.

If $L_{f2} = L_{f1}$, $V_{TCM} = V_{CM} = V_{cpv}$. Hence, the Common mode leakage current

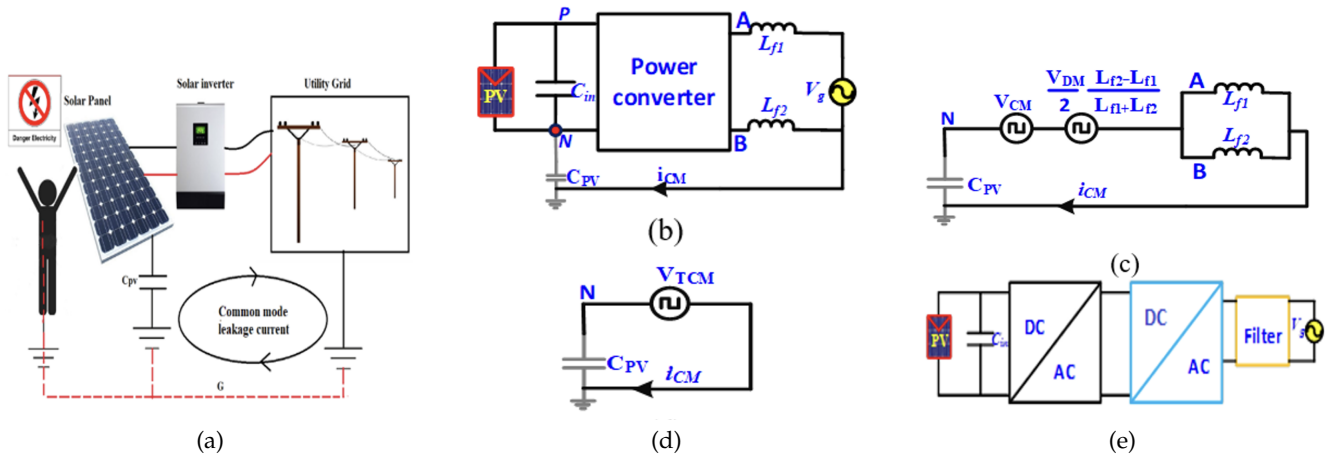


Fig. 1. (a) CMLC Effect (b) Configuration of TLI (c)Common mode model of TLI (d) Reduced common-mode model (e) General structure of Pseudo-DC link inverter

$$i_{CM} = i_{CPV} = C_{PV}\frac{dV_{CM}}{dt} \tag{2}$$

Eq. (2)) indicates that maintaining the constant common-mode voltage (CMV) mitigates the CMLC. Neutral point grounding, double grounding, Bipolar PWM, DC-decoupling, and AC-decoupling are the various methods used to mitigate the leakage current. By connecting the DC-side neutral point and grid neutral, CMV is maintained at DC-link capacitor voltage. However, a neutral point grounded inverter requires dual input voltage [5]. Most of the double grounded inverters use the virtual DC bus and switched capacitor structure. The double grounding technique connects the PV ground to grid neutral, which short circuits the PV ground capacitance, and eliminates CMLC. Nevertheless, the virtual DC bus structure reduces PV utilization [6], and the switched-capacitor raises the current stress [7] Bipolar PWM is the simplest technique, which maintains constant CMV. Nonetheless, the two-level output of Bipolar PWM increases the voltage stress across the switches and total harmonic distortion (THD) [8]. The decouple switches of DC decoupled inverters are opened during the zero states to decouple the grid and PV panel [9]. Though this decoupling reduces the CMV oscillations, the conduction of additional switches during the active states increases the conduction loss. The AC-decoupled inverters have decoupled switches on the AC side, which conduct during the zero states. Hence, the AC decoupling method is used in the proposed inverter, which reduces the conduction loss [10]. The TLI, which don't have boosting ability should have high input voltage rating. Else, they are connected to DC-DC converter and operated in two stages [9]. The two-stage operation increases the size, cost, and losses [11]. Many soft switching-based inverters [12, 13] have complicated structures but don't have boosting ability. Unlike the two-stage inverters, single-stage inverters do the boosting and DC to AC conversion in single-stage operation. Though the single-stage inverters have reduced size, they have poor power quality, less boosting ability, and in-equal power-sharing [14]. Semi-two stage inverters [15, 16] operate in two stages whenever PV voltage is lesser than grid voltage and work in single-stage during the remaining period. As, two-stage operation is performed whenever required, the efficiency is improved. Nevertheless, the changeover from one stage to another stage distorts the grid current. Also, semi-two stage inverters need additional switches to add and remove the boosting stage. The pseudo-DC link type inverter overcomes the disadvantages of single-stage, two-stage, and semi-two-stage inverters. The general structure of pseudo-DC link inverters is shown in Fig. 1(e). They don't need a DC-link capacitor between the boosting and inverter stages. Thus the proposed inverter has reduced leakage current, high boosting ability, and doesn't need a DC-link capacitor.

2. Proposed inverter

2.1. Topology structure

The structure of proposed topology (Fig. 2(a)) has a high gain boosting stage [17] coupled with an AC-decoupled inverter [18]. Boosting stage is colored in light blue, and decouple switches are colored in purple. The H-bridge with filter structure is colored in black. The switching pulses are shown in Fig. 2(b). The triangular carrier signal is compared with the sinusoidal modulating signal to generate the pulses of S_1-S_5. Carrier signal is compared with a constant

reference signal to generate the pulses of S_6-S_7.

The modulation ratio ($M=A_m/A_c$) should be lesser than duty cycle ($D= A_r/A_c$). In the following analysis, the instantaneous and steady-state or average variables are represented in lower case and upper case letters, respectively.

2.2. Modes of operation

2.2.1. Active state-I and III

During the positive half cycle active state-I and negative half cycle active state-III, inductors L_1 and L_2 are charging through S_6 and S_7 (Fig. 3(a) and (c)). The PV and charged capacitors (C_1, C_2) are supplying the grid. During the positive half cycle, S_1 and S_2 connect the virtual DC bus to the grid (Fig. 3(a)). Whereas, during the negative half cycle, S_3 and S_4 conduct to connect the virtual DC bus to grid Fig. 3(c). The dynamic equations during the active states are given in Eq. (3)-(7).

$$\text{Input current } i_{in} = i_{L1} + i_{L2} + i_{dc} \tag{3}$$

Let inductor L_1=L_2= L; hence i_{L1}=i_{L2} = i_{IND}

$$\text{Hence } i_{in} = 2i_{IND} + i_{dc} \tag{4}$$

Let voltage across the inductor v_{L1}=v_{L2}=v_L

$$\text{Input voltage } v_{in} = v_L \tag{5}$$

The closed loop voltage equation

$$V_{in} + V_{c1} - V_{dc} + V_{c2} = 0 \tag{6}$$

Let the voltage across capacitor v_{c1}=v_{c2}=v_C Hence,

$$v_c = (v_{dc} - v_{in})/2 \tag{7}$$

2.2.2. Zero state-II and IV

During the zero states, the inductors L_1 and L_2 are discharging through the diodes D_1 and D_2 to charge the capacitors C_1 and C_2. During the positive half cycle, the filter inductors are discharging through D_3, S_5, and D_4 to produce the zero voltage. Whereas, during the negative half cycle, the filter inductors are discharging through D_5, S_5, and D_6 to make the zero voltage. The dynamic equations during the zero state is given in Eq. (8)-(10). Let the current through capacitor i_{c1}=i_{c2} = i_C

$$i_{in} = i_{IND};\ \text{Hence } i_c = i_{IND}/2 \tag{8}$$

$$V_{in} + v_{L2} - v_{c2} - v_{L1} = 0 \tag{9}$$

$$V_L = (V_{in} - v_c)/2 \tag{10}$$

2.3. Steady-state analysis

The inductor voltage-second balance equation is given in Eq. (11);

$$V_{Lavg} = \frac{1}{T_s}\left((DT_s\,(V_{in})) + ((1-D)T_s)\left(\frac{V_{in}-V_c}{2}\right)\right) = 0 \tag{11}$$

Where T_s refers to the switching period. The average inductor voltage

$$V_c = V_{in}\left(\frac{1+D}{1-D}\right) \tag{12}$$

By substituting Eq. (7) in the Eq. (12), Eq. (13) was obtained.

$$\frac{V_{dc}-V_{in}}{2} = V_{in}\left(\frac{1+D}{1-D}\right) \tag{13}$$

$$V_{dc} = V_{in}\left(\frac{3+D}{1-D}\right) \tag{14}$$

Thus, boosting stage gain (B) is expressed in Eq. (15)

$$B = \frac{V_{dc}}{V_{in}} = \left(\frac{3+D}{1-D}\right) \tag{15}$$

The modulation index and the output peak voltage are represented as M and V_{acp}, respectively. The overall inverter gain (G) is derived in Eq. (17).

$$G = \frac{V_{acp}}{V_{dc}} \cdot \frac{V_{dc}}{V_{in}} \tag{16}$$

$$G = M.B = M.\left(\frac{3+D}{1-D}\right) \tag{17}$$

Using the dynamic input current equations Eq. (4) and Eq. (8), the average input current (I_{in}) is derived in Eq. (18).

$$I_{in} = \frac{1}{T_s}\left((DT_s\,(2I_{IND} + I_{dc})) + ((1-D)T_s)\,I_{IND}\right) \tag{18}$$

$$I_{IND} = (I_{in} - DI_{dc})/(1+D) \tag{19}$$

Eq. (20) is obtained by neglecting the losses.

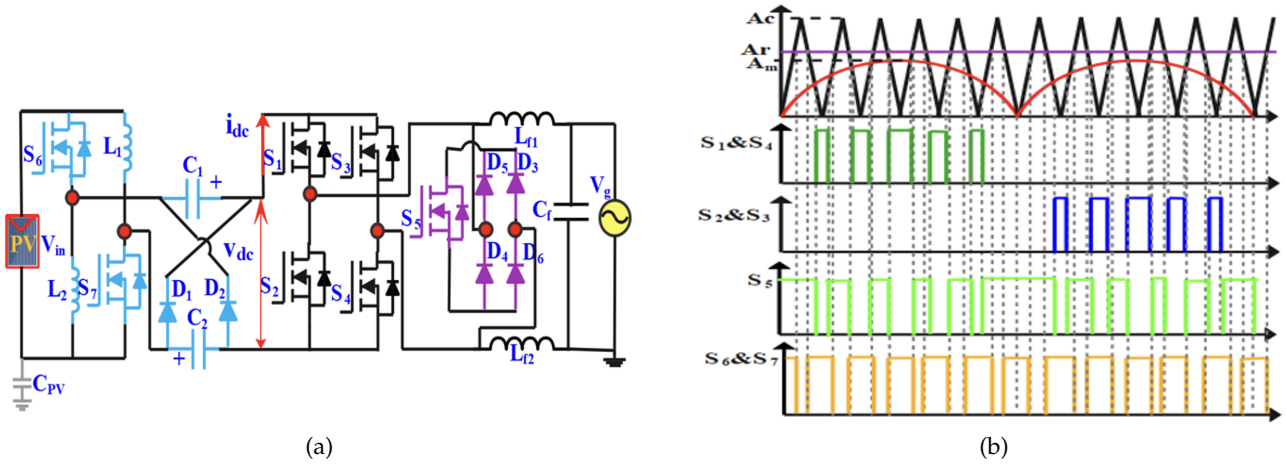
$$P_{in} = P_{DC} = P_0 \tag{20}$$

Where, P_{in}, P_{DC} and P_o represent the input power, power at fictitious DC bus and output power respectively. Hence,

$$V_{in}I_{in} = V_{dc}I_{dc} = V_{ac}I_{ac} = P_o \tag{21}$$

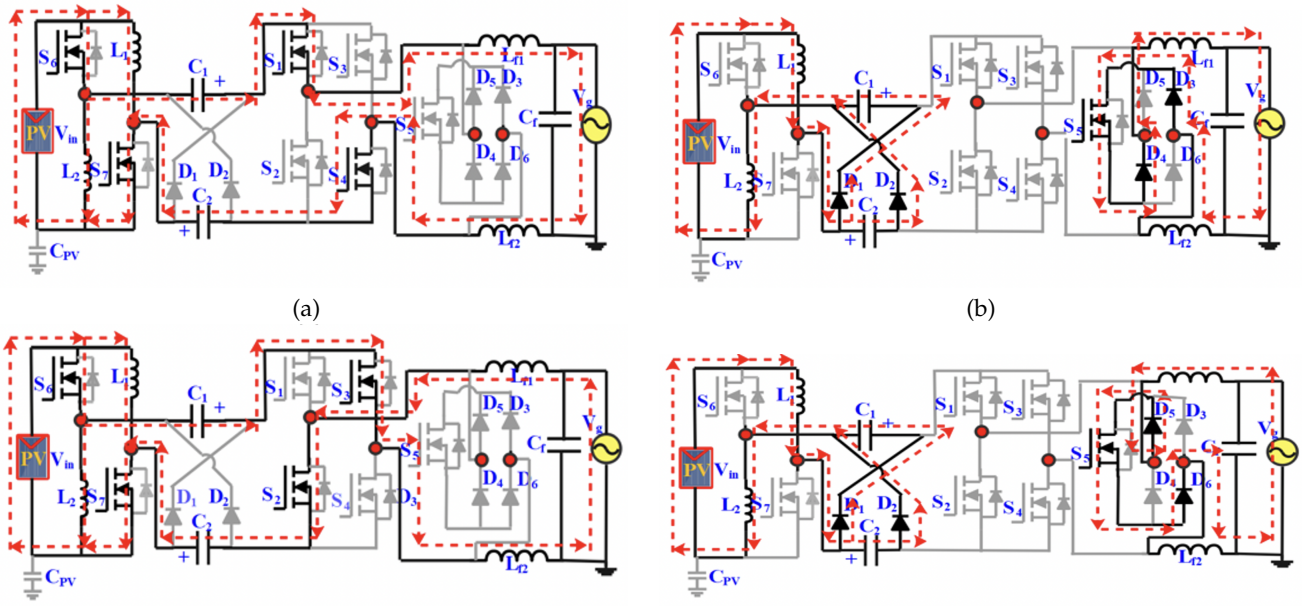
Using Eqs. (15) and (21), Eq. (22) was derived.

$$V_{in}\left(\frac{3+D}{1-D}\right)I_{dc} = V_{in}I_{in} \tag{22}$$



(a) (b)

Fig. 2. (a) Structure of proposed topology (b) Switching pulses



(a) (b)

(c) (d)

Fig. 3. (a) Positive half cycle active state-I (b) Positive half cycle zero state-II (c) Negative half cycle active state-III (d) Negative half cycle zero state-IV

$$I_{dc} = \frac{P_O(1-D)}{V_{in}(3+D)} \quad (23)$$

Inductor current (I_{IND}) is obtained by substituting Eq. (23) in Eq. (19).

$$I_{IND} = \frac{P_O\left(3+D^2\right)}{V_{in}\left(3+4D+D^2\right)} \quad (24)$$

3. Design of inductors and capacitors

The boosting inductor design depends on the average inductor current and boosting capacitor design depends on the average capacitor voltage.

3.1. Design of L_1 and L_2

From Eq. (5),

$$V_{in} = \frac{L\Delta I_{IND}}{DT_s} \quad (25)$$

Hence, inductor

$$L_1 = L_2 = L = \frac{V_{in}D}{\Delta I_{IND} f_S} \quad (26)$$

The inductor current ripple, ΔI_{IND}, can be 10% to 20% of inductor current obtained in Eq. (24)

3.2. Design of C_1 and C_2

The average capacitor current during the discharging period (I_c) is attained from Eq. (8).

$$Ic = \frac{C\Delta V_C}{(1-D)T_s} = \frac{I_{IND}}{2} \quad (27)$$

$$\text{Capacitor}\, C_1 = C_2 = C = \frac{I_{IND}(1-D)}{2\Delta V_C f_s} \quad (28)$$

ΔV_c can be 10% to 20% of V_c inductor current obtained in Eq. (12)

3.3. Design of filter

The filter components L_f and C_f can be designed using Eq. (29)-(32) [19]. Peak ripple factor ($\Delta I_{Lf\,factor}$))is obtained as 0.24. The current ripple in an inductor might range from 20% to 40% of the rated inductor current.

$$\Delta I_{Lf\,factor} = M\sin(2\pi ft) + M^2\sin^2(2\pi ft) \quad (29)$$

Minimum value of filter inductor

$$L_{fmin} = \frac{\Delta I_{Lf\ factor} * v_g}{f_s * \Delta I_{Lf}} \quad (30)$$

$$C_f = \frac{1}{(2\pi f_c)^2\ L_f} \quad (31)$$

$$10\%\ \text{of}\ f_s \ll \text{cutoff frequency}\ (f_c) \ll \frac{fs}{2} \quad (32)$$

where, f_s and f_s represent the switching frequency and carrier frequency, respectively.

Table 1. Simulation parameters-MATLAB

Simulation Parameters	Value
Input voltage-V_{in}	30V
Output voltage (RMS)-V_{ac}	220V
Rated power	200W
Load-R_L	250 Ω
Switching frequency-f_s	50kHz
Grid frequency-f	50Hz
Ground resistance	5 Ω
Capacitors –C_1,C_2	50µF
Inductors –L_1,L_2	220µH
Filter inductors –L_{f1},L_{f2}	3mH
Filter capacitor –C_f	0.3µf
Duty cycle-D	0.75
Modulation Index-M	0.74
Parasitic capacitance-C_{PV}	50nF

4. Simulation analysis

The proposed inverter is simulated using MATLAB Simulink with the parameters given in Table 1. The input voltage and duty cycle are set as 30V (Fig. 4(a)) and 0.75, respectively. According to Eq. (15), the input voltage is boosted to peak fictitious DC bus voltage of 450V (Fig. 4(a)). The current through inductor L1 with its zoomed view are shown in Fig. 4(b). The boosting stage gain(B) under varying input voltage condition is shown in Fig. 4(c).

The inverter output voltage sensed at the bridge arm terminals (v_{acwo}), the load voltage (v_{ac}), and current through the load (i_L) are shown in Fig. 5(a). The output voltage and current under varying input voltage condition is shown in Fig. 5(c). The THD of the load current Fig. 6(a) is measured as 1.82%, which satisfies the standard IEEE519 (<5%). The voltage across the parasitic capacitance (v_{cpv}) and the CMLC are shown in Fig. 5(b). As the PV panel capacitance (C_{PV}) varies with climatic conditions, CMLC is measured with varying PV panel capacitance (50-250 µF). The measured RMS value of CMLC (Fig. 6(b)) is lesser than 35mA, which is far below the standard VDE0126-1-1 (<300 mA). Therefore, the proposed topology is appropriate for standalone and grid-connected applications.

The duty cycle (D) and modulation index (M) are varied with the varying input voltage conditions (24V-295V) to produce the output voltage (V_{ac}) of 220V (Fig. 4(d)). Hence, the proposed topology is applicable for PV integrated applications.

5. Loss and thermal analysis of proposed inverter

The thermal analysis is done in PLECS platform with the parameters given in Table 2. The electrical-thermal model is shown in Fig. 7(a)[20]. The turn-on loss, turn-off loss, conduction loss, and thermal impedance parameters of the

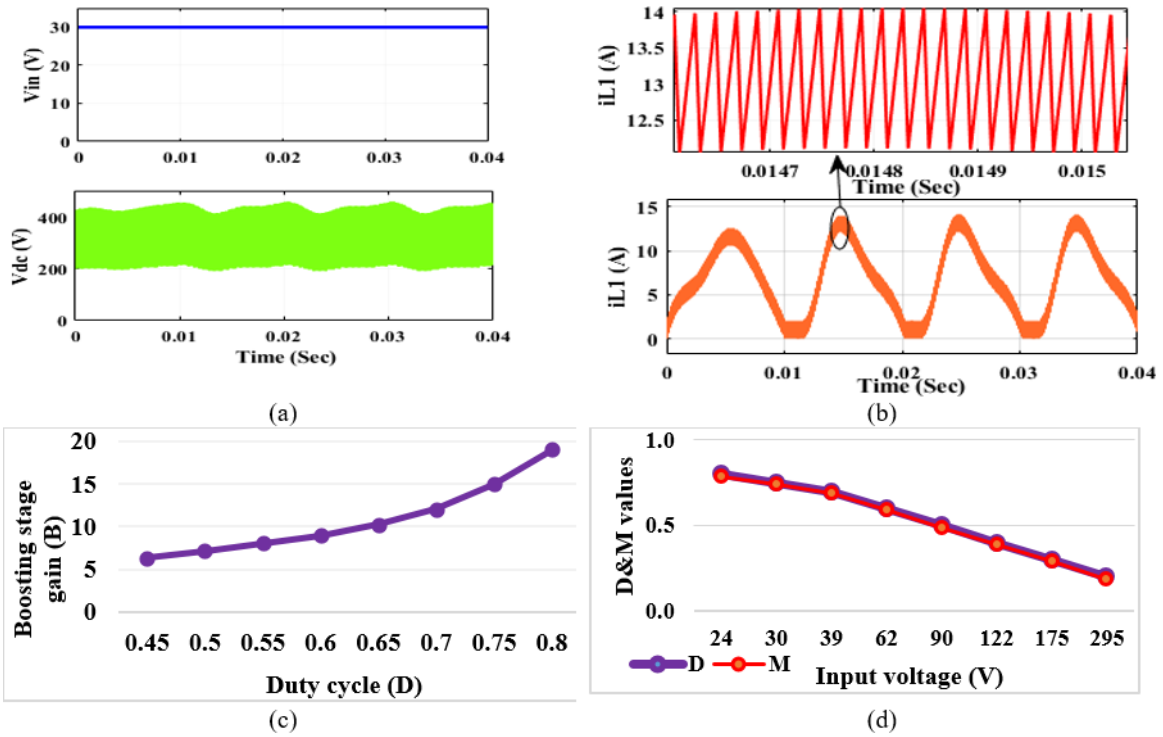


Fig. 4. (a) Input voltage (vin) and DC bus voltage (vdc) (b) Inductor current with zoomed view (c) Boosting stage gain (B) with varying input voltage (d) Duty cycle (D) and Modulation index (M) with varying input voltage

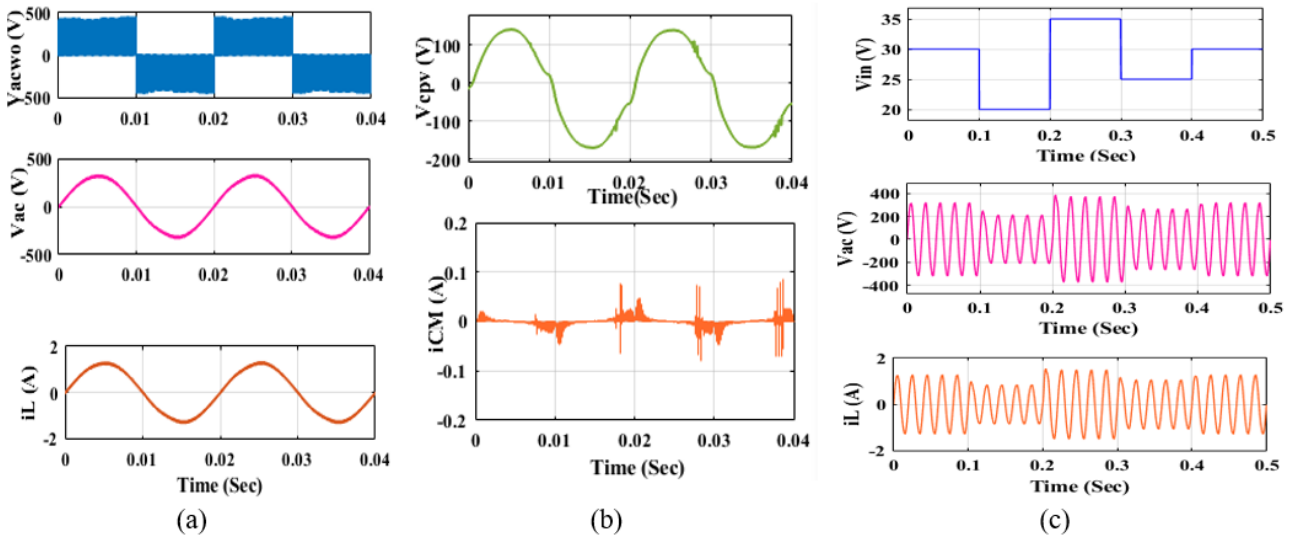


Fig. 5. (a) Voltage measured before filter (vacwo), Load voltage (vac) and Load current (iL) with 30V input. (b) Voltage across PV panel capacitance (vcpv) and CMLC (iCM) with 30V input (c) Load voltage and current with varying input voltage under standalone condition

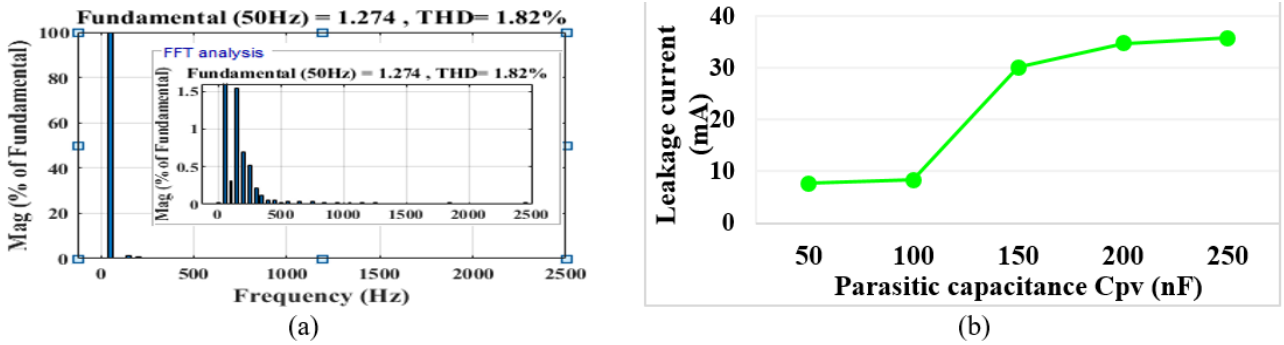


Fig. 6. (a) Load current THD (b) CMLC with varying C_{pv}

Table 2. Simulation parameters-PLECS

Simulation Parameters	Value
Si-IGBT(S7&S8)-SEMIKRON100GB125DN	UCE=1200V, Ic=100A
SiC-MOSFET(S7&S8)-IMW120R030M1H	UDS=1200V, ID=56A
SiC-MOSFET(S1-S6)-IMW120R350M1H	UDS=1200V, ID=4.7A
Diode-IGB15N60T	UFWD=600V, IFWD=15A
Si-IGBT(S1-S6)-IKW08N65H5	UCE=650V, Ic=8A
GaN-MOSFET(S7&S8)-GS61008	UDS=100V, ID=90A
GaN-MOSFET(S1-S6)-GS065008	UDS=650V, ID=8A
Worst case heat sink temperature-Tworst	120°C
Ambient temperature	40°C

switches are fed into PLECS [21–23]. As a sample, the loss parameters of SEMIKRON switches are shown in Figs. 7 and 8. T_{Hworst} is the peak heat sink temperature, which is below the switch-junction temperature limit. $P_{lossworst}$ is the loss measured at T_{Hworst}. The thermal resistance (R_{th}) is calculated by Eq. (33). PLECS calculates the total switch loss (P_{Sloss}) using the Eq.(33)-(37), by locating the Rth in the thermal model. The controlled switch (MOSFET or IGBT) is referred as switch here.

$$R_{th} = \frac{T_{Hworst} - T_{amb}}{Plossworst} \tag{33}$$

$$\text{Total switch loss-}(P_{Sloss}) = P_{CS} + P_{SS} + P_{CFWD} + P_{RRFWD} \tag{34}$$

where, P_{CS}, P_{SS}, P_{CFWD} and P_{RRFWD} are the conduction loss of the switch, switching loss of the switch, conduction loss of the freewheeling diode and reverse recovery loss of the freewheeling diode.

$$\text{Conduction loss of switch-}P_{CS}(t) = V_{on}(t).i_{on}(t) \tag{35}$$

Where, V_{on} represents the collector-emitter or drain-source voltage and ion represents the collector or drain current during the on period.

$$P_{CFWD}(t) = V_{FWDon}(t).i_{FWD}(t) \tag{36}$$

Where, V_{FWDon} and i_{FWD} represent the forward voltage of the freewheeling diode and forward current of the freewheeling diode, respectively.

$$P_{RRFWD}(t) = (1/4).Q_{RR}.V_{FWDRR} \tag{37}$$

Where, Q_{RR} and V_{FWDRR} represent the reverse recovery charge and freewheeling diode voltage during the reverse recovery period, respectively. PLECS computes the diode loss (P_{Dloss}) like the freewheeling diode loss given in Eqs. (36) and (37). The thermal loss of the inverter ($P_{thermal\,loss}$) is calculated using the Eqs. (38) to (41).

$$P_{thermallosses} = \sum_i P_{Sloss} + P_{Dloss} \tag{38}$$

Total loss of the inverter (P_{total}) is calculated using the Eq. (39).

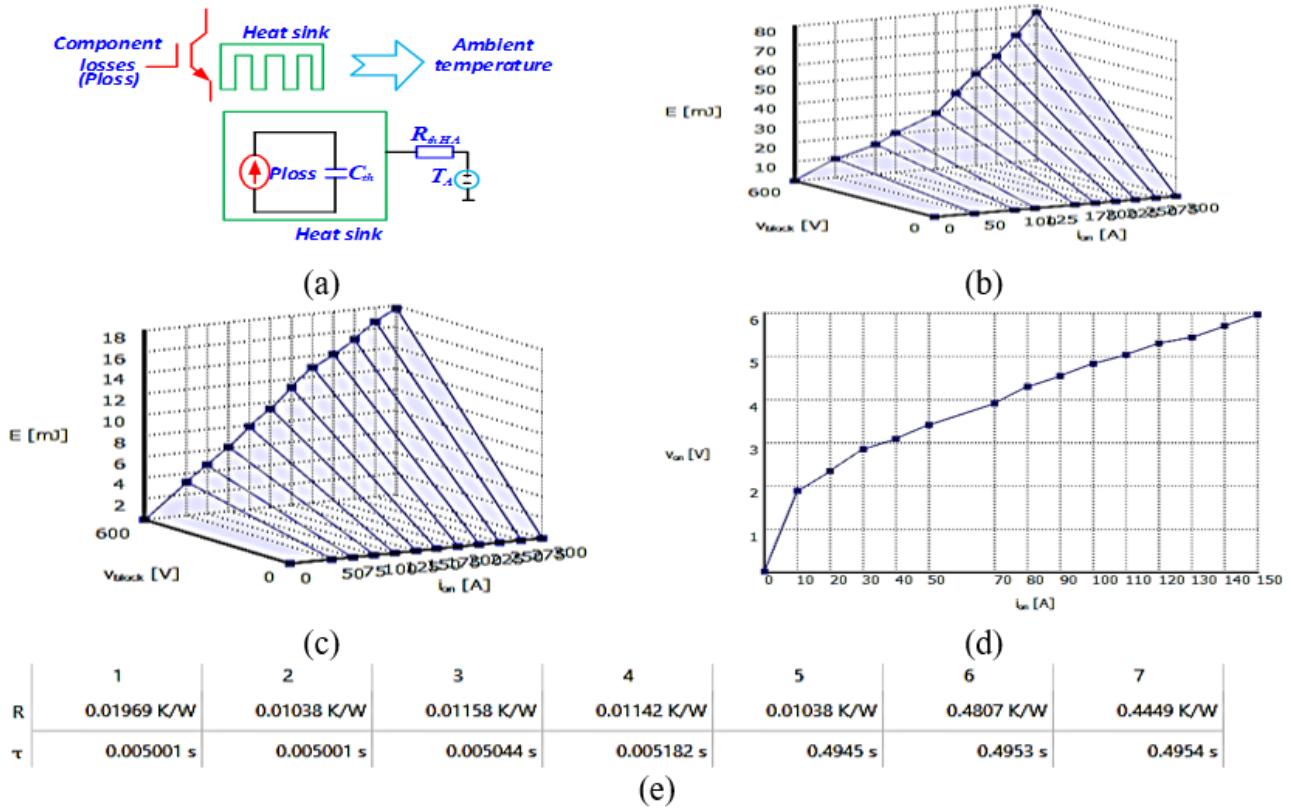
$$P_{total} = P_{thermallosses} + P_L + P_C \tag{39}$$

Where, P_L and P_C represent the inductor's conduction loss and capacitor's conduction loss, respectively.

$$P_L = I^2_{LRMS}.R_{LDC} \tag{40}$$

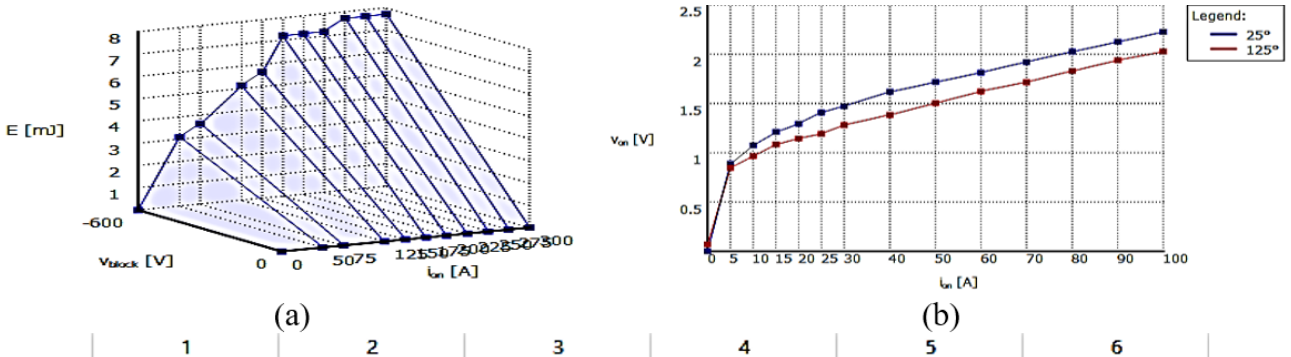
$$P_C = I^2_{CRMS}.R_{CESR} \tag{41}$$

Where, I_{LRMS}, R_{LDC}, I_{LRMS} and R_{CESR} represent the RMS value of inductor current, DC resistance of inductor, RMS value of capacitor current and equivalent series resistance of capacitor, respectively.



	1	2	3	4	5	6	7
R	0.01969 K/W	0.01038 K/W	0.01158 K/W	0.01142 K/W	0.01038 K/W	0.4807 K/W	0.4449 K/W
τ	0.005001 s	0.005001 s	0.005044 s	0.005182 s	0.4945 s	0.4953 s	0.4954 s

Fig. 7. (a) Electrical thermal model; Silicon made SEMIKRON Switches S_7-S_8 (b) Turn-on loss (c) Turn-off loss (d) Output characteristics-Conduction loss (e) Thermal impedance characteristics



	1	2	3	4	5	6
R	0.01827 K/W	0.01827 K/W	0.01827 K/W	0.0823 K/W	0.2718 K/W	0.9583 K/W
τ	0.005001 s	0.005001 s	0.005001 s	0.005001 s	0.5226 s	0.84 s

(c)

Fig. 8. Silicon made SEMIKRON Freewheeling diode S_7-S_8 (a) Reverse recovery loss (b) Output characteristics-Conduction loss (c) Thermal impedance characteristics

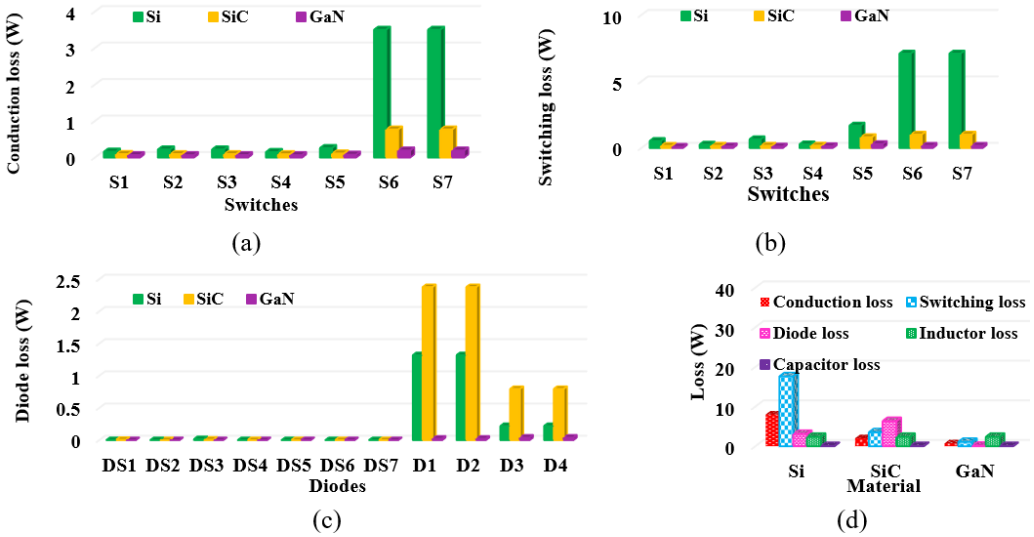


Fig. 9. (a) Conduction loss of switches (b) Switching loss of switches (c) Diode & anti-parallel diode losses (d) Contribution of losses

The calculated losses of the inverter made of Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN) switches with the parameters in Table 1 are compared in Fig. 9(a)-(d). GaN devices have lesser conduction loss (Fig. 9(a)), as the on-resistance of GaN devices is lesser than Si and SiC materials [24]. The internal capacitances of GaN switches offer lower turn-on loss, (Fig. 9(b)). As GaN switches don't have an anti-parallel diode, they don't have body diode loss (Fig. 9(c)).

$$\text{Efficiency } \eta = \frac{P_{input} - P_{total}}{P_{input}} \tag{42}$$

$$\eta_{CEC} = (0.04 * \eta_{10\%}) + (0.05 * \eta_{20\%}) + (0.12 * \eta_{30\%}) + (0.21 * \eta_{50\%}) + (0.53 * \eta_{75\%}) + (0.05 * \eta_{100\%}) \tag{43}$$

$$\eta_{EU} = (0.03 * \eta_{5\%}) + (0.06 * \eta_{10\%}) + (0.13 * \eta_{20\%}) + (0.1 * \eta_{30\%}) + (0.48 * \eta_{50\%}) + (0.2 * \eta_{100\%}) \tag{44}$$

The efficiency comparison at different power is calculated using Eq. (42) and shown in Fig. 10(a). The California Energy Commission efficiency (η_{CEC}) and the European efficiency (η_{EU})are calculated using the Eqs. (43) and (44), which are also enhanced with GaN manufactured switches (Fig. 10(c)). The efficiency comparison at different power is shown in Fig. 10(a). The modulation index (M) is varied with varying input voltage to attain the same rated power. If the input voltage increases, the current drawn from the source reduces, which reduces the inverter's losses (Fig. 10(b)). PLECS calculates the switch junction temperature (T_{JS}), diode junction temperature (T_{JD}) and heat sink-temperature (T_H) using the Eqs. (45) to (49).

$$T_{JS}(t) = \left(P_{Sloss}(t) * Z_{SthJC}(t)\right) + T_C(t) \tag{45}$$

$$T_{JD}(t) = \left(P_{Dloss}(t) * Z_{DthJC}(t)\right) + T_C(t) \tag{46}$$

$$T_H(t) = (P_{Dloss}(t) + P_{Sloss}(t)) * Z_{Hth}(t) + T_A \tag{47}$$

Where, Z_{thJC}, T_A are the junction to case thermal impedance and ambient temperature, respectively.

$$Z_{thJC}(t) = \sum_{i=1}^{n} R_{thi} * \left(1 - e^{\frac{-t}{\tau_i}}\right), \text{ where } \tau_i = R_{thi} * C_{thi} \tag{48}$$

$$1/C_{th} = T_j/Q \tag{49}$$

Where, τ_i, Q and C_{th} represent the time constant, flowing heat in time 't' and thermal capacitance, respectively.

The temperature rise of inverter with different materials are shown in Fig. 11(a)-(c), which infers that the higher thermal conductivity of GaN material reduce its temperature rise. The nominal temperature rise of the inverter proves that the inverter can operate with a nominal heat sink. Table 3 proves that the proposed topology has higher gain, makeing it to operate in wide input voltage range. Unlike two-stage and semi-two stage inverters, this topology don't require a DC-link capacitor [25].

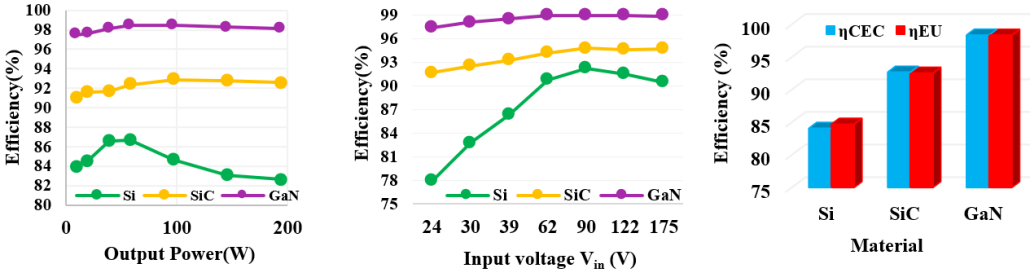


Fig. 10. (a) Efficiency at varying power (b) Efficiency at rated power (200W) with varying V_{in} (c) Weighted efficiency

Table 3. Comparison of existing topologies with proposed topology

Topology name	NS	ND	NL	NC	G	G- Rating	Filter	Reported advantages	Limitations
Semi two stage multilevel [16]	12	2	3	2	M/(1-D)	Medium	LCL	Less THD, Less current stress	Increased size, Less voltage gain, Complicated PWM with multiple references
Integrated Boost [15]	9	1	1	1	M/(1-D)	Medium	L-L	Semi two-stage reduces losses.	Leakage current is beyond the limit, and output current is distorted during the transition from single to two-stage, Less voltage gain.
HB buck-boost [5]	4	0	1	0	NA	Very less	L	Fewer components	Double input voltage requirement, More than one PV sources create grid current distortion.
Switched capacitor 5level [7]	6	2	0	1	2	Less	L	Less switching loss, iCM=0	Higher voltage &current stress, Less voltage gain
Bidirectional buck- boost [14]	6	0	1	0	NA	Less	LCL	No additional decouple switches, iCM=0	Need of energy balance of input capacitors, Less voltage gain
ZVT [12]	8	3	2	2	No Boost	No Boost	LC	Mitigation of switching loss, Compact resonant circuit	Interaction between resonant circuits, Risk of saturation of resonant inductors
Proposed-Topology	7	6	2	2	M(3+D)/(1-D)	Very high	LCL	Very high gain, Wide input voltage Range , Reduced leakage current.	Additional decouple switches and diodes

**N_S-Number of controlled switches, N_D- Number of diodes, N_L-Number of inductors excluding filter inductors, N_C-Number of capacitors excluding filter and DC link capacitors, G-overall Voltage gain i_{CM}-Common mode leakage current, NA-Not available

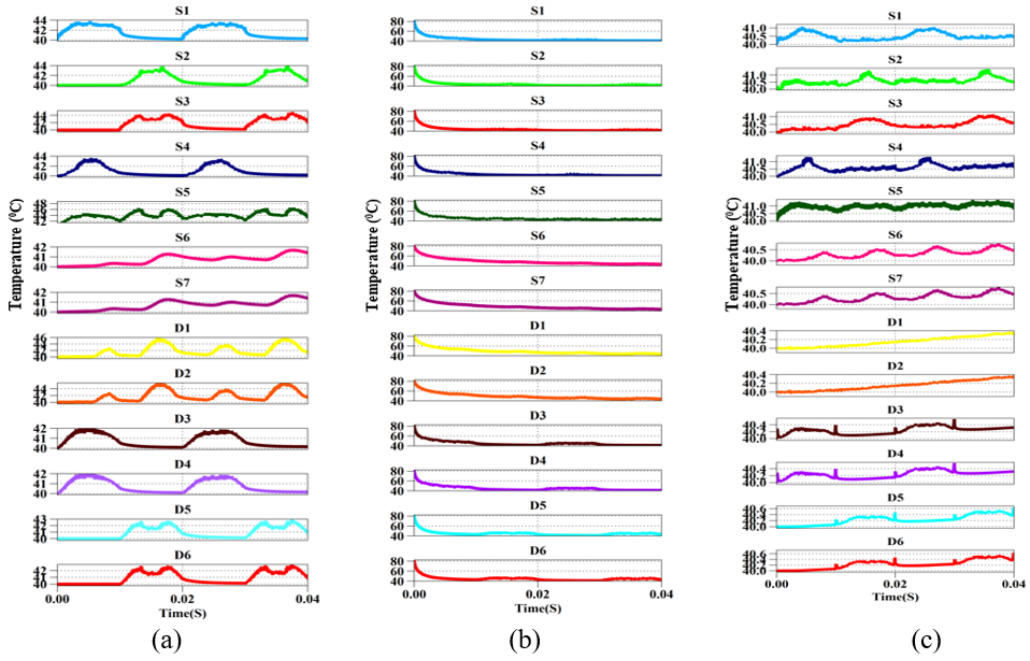


Fig. 11. Junction temperature of components– (a) Si-made (b) SiC-made (c) GaN-made

6. Conclusion

This paper proposes a new Pseudo-DC link type AC-decoupled inverter. The modes of operation, design and steady-state analysis of the proposed topology are elaborated. The simulated results of the proposed inverter infer that the topology can work with a wide input voltage range (24V to 295V). Hence, the proposed inverter is suitable for PV integrated applications. As the measured RMS value of leakage current is less than 35mA for varying PV panel capacitance, the proposed inverter is suitable for grid-connected applications. The loss contribution of the inverter made of three different materials(Si, SiC, and GaN) are compared. The inverter attains the efficiency of 82.63%, 92.56%, and 98.09%, with Si, SiC and GaN made switches, respectively at a rated power of 200W and 30V input. When the input voltage is increased, the proposed inverter can reach the maximum efficiency of 92.26%, 94.81%, and 98.96% with Si, SiC and GaN made switches, respectively. Thus, the proposed topology with evolving SiC and GaN made devices offer higher efficiency.

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