Z Source Inverter With High Gain Improved Switched Inductance

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Aiming at the problems such as small boost gain, large start-up shock, low DC side voltage utilisation, high current-voltage harmonic distortion rate, etc. of the conventional Z-source inverter (ZSI), which can not be well applied in new energy generation situations, the Zimpedance source network is improved. A Z-source inverter with high gain improved switched inductance (HISL-ZSI) topology is proposed. The HISL-ZSI topology is based on the switched-inductor Z-source inverter (SL-ZSI) with an inductor and active switch behind its DC source to form a BOOST circuit with the front stage, further improving the boost capability. A high boost unit is formed with a modified switching inductor module in the back stage, and the capacitive voltage stress on the device is reduced under the same conditions. Furthermore, the addition of the inductor behind the DC source makes the input current continuous, improving the service life of the DC source and the DC side voltage utilisation. On the basis of theoretical analysis, a simple boost control modulation strategy is used to simulate the system using Matlab/Simulink. Simulation results show that the HISL-ZSI topology has superior boosting capability, reduces capacitive voltage stress and ensures continuous input current, making the HISL-ZSI better suited for use in new energy generation applications.

Keywords: Booster capacity; Capacitive voltage stress; Improved topology; New energy power generation; Z-source inverter

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1. Introduction

As a new type of energy, solar energy and wind energy have attracted more and more attention by virtue of their pollution-free, renewable and other advantages [1]. In photovoltaic and wind power generation systems, the DC input voltage varies in a wide range due to the interference of environment and other factors [2]. In order to interconnect new energy generation systems to the grid, and to improve the quality of electricity generated by new energy sources. It is necessary to have grid-connected inverters with a stable performance and a wide range of voltage ramping. However, conventional voltage and current inverters suffer from the following problems: the output voltage is lower than the DC input voltage for step-down inverter, the "dead zone" causes the output current distortion, and the upper and lower bridge arms are switched on at the same time, resulting in short circuit damage to the inverter and other defects, which cannot meet the requirements of new energy system grid-connection [3]. Therefore, it is necessary to overcome these problems with a new inverter with a wide range of ups and downs.

In 2003, Peng Fangzheng first proposed Z-source inverter (ZSI) [4], The proposed ZSI overcomes the defects of the traditional voltage source inverter and greatly improves the input voltage range. The circuit topology uses the Z-shaped impedance source network (Z-source) to make the through state prohibited by the traditional voltage type inverter become its normal state, and uses the through state to improve the DC input voltage of the inverter, so it can be applied in the new energy power generation [5].

In addition, ZSI can be widely used in other new energy applications, For example, literature [6] applies ZSI to AC speed control systems, literature [7] uses ZSI for motor drive control, literature [8] Study of single uninterruptible power supply based on the merits of ZSI, literature [9] proposes a fixed frequency controller to control the duty cycle of a passthrough, thus, it can be effectively used in electric vehicles, literature [10] investigated the application of ZSI in traction drive of fuel cell-battery hybrid electric vehicles. However, ZSI still has some shortcomings, such as limited voltage boost range, capacitor voltage stress, etc [11], In order to overcome the above shortcomings, many scholars have carried out in-depth research on the new topology based on traditional ZSI. Depending on the impedance components (inductor arrangement), energy storage quasi-Z-source inverters have been proposed in literature [12] and current quasi-Z-source inverters have been proposed in literature [13]. They preserve the advantages of conventional ZSI with less capacitive voltage stress. However, the output gain is still small and cannot meet the demand of new energy generation. The new voltage doubling ZSI proposed in literature [14] combines two double-loop voltage doubling units and shares a coupling inductor. This topology has a high voltage boost factor and is suitable for occasions with high voltage range requirements. Literature [15] proposes an improved voltage type ZSI, which uses two transformers to replace two inductors in the ZSI impedance source network. Compared with T-Z source inverter, this inverter can obtain higher voltage gain with lower turns ratio, thus saving cost. However, the overall cost is still high and the capacitive voltage stress is high.

The SL-ZSI proposed in literature [16] greatly improves the boost gain of the impedance source network, but the capacitor voltage stress is larger when the boost multiple is large. The enhanced ZSI proposed in the literature [17] replaces the inductive element in the Quasi-ZSI with two switching inductor modules to obtain a higher boost gain, but with a consequent increase in capacitive voltage stress. Others have replaced the traditional two-level ZSI with a three-level ZSI to reduce its harmonic distortion rate and capacitive voltage stress [18]. Literature [19, 20] proposed an improved three-level ZSI, which can realize bidirectional power transmission and has a wider application range, reducing the capacitor voltage stress, but the output waveform has a high harmonic content, and the phenomenon of midpoint potential drift occurs. The novel three-level inverter proposed in literature [21] further improves the booster capacity of the inverter, but increases the number and complexity of the devices, and increases the difficulty and cost of control. The five-level quasi-Z-source inverter proposed in literature [22]. It has a large boost capacity and a small harmonic distortion rate of voltage and current, but the cost is high. The high voltage gain quasi impedance source coupled inductor multilevel inverter proposed in literature [23], the five-level six-switch coupled Q-ZSI inverter proposed in this paper has fewer passive components, higher voltage boost capacity, but higher capacitor voltage stress.

Based on existing research, a modified switched inductive Z-source inverter (HISL-ZSI) topology with high gain is proposed in this paper. It is based on the switched-inductor Z-source inverter (SL-ZSI) by adding an inductor and active switch behind the DC source to form a BOOST circuit with the front stage, forming an impedance source network with higher gain and ensuring continuous input current due to the addition of the inductor. Compared to other typical topologies [24–26], the HISL-ZSI topology proposed in this paper has the following advantages:

1. further boosting capability;
2. less stress on the passive devices with the same boosting gain; and
3. guaranteed continuous input current at start-up, improving the utilisation of the DC source.

2. Switched inductor z-source inverter

The switched inductor Z-source inverter topology is shown in Fig. 1. This topology replaces the inductive components in a conventional Z-source inverter with switched inductor modules, effectively increasing the boost factor of the Z-source network. As with the ZSI, the SL-ZSI also has two modes of operation, straight-through and non-straight-through as shown in Fig. 2.

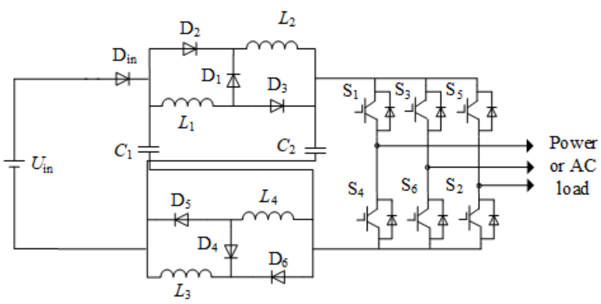
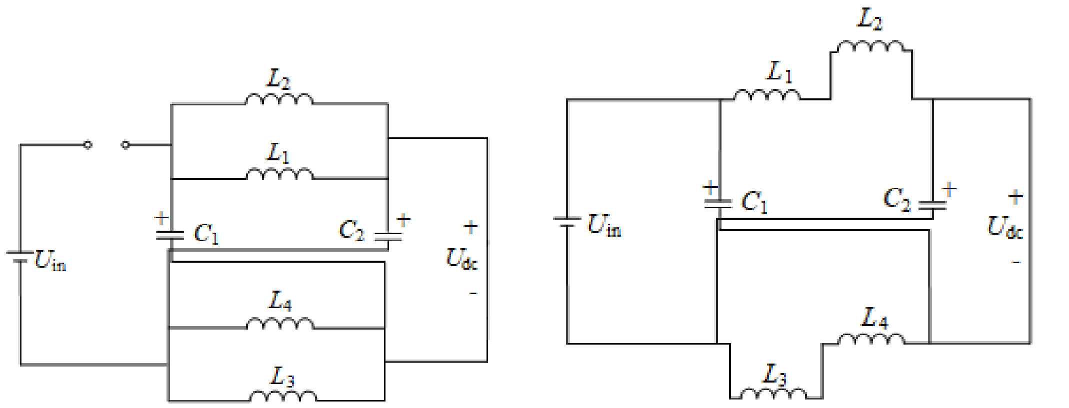


Fig. 1. SL-ZSI topology

From the literature [16], let T be the switching period, T_0 be the pass-through time, and the pass-through duty cycle $D = T_0/T_{\text{then}}$, the boost factor B of the SL-ZSI network is:



(a) Equivalent circuit diagram of through state (b) Equivalent circuit diagram of non-through state

Fig. 2. SL-ZSI equivalent circuit

$$B = \frac{1+D}{1-3D} = \frac{1+(T_0/T)}{1-3(T_0/T)} \tag{1}$$

The capacitor voltage stresses U_{C1} and U_{C2} are:

$$U_{C1} = U_{C2} = \frac{1-D}{1-3D}U_{\text{in}} \tag{2}$$

The relationship between the DC bus voltage U_{dc} and U_{in} is given by:

$$U_{\text{dc}} = BU_{\text{in}} = \frac{1+D}{1-3D}U_{\text{in}} \tag{3}$$

If the modulation factor of the inverter is M, the peak inverter output phase voltage is:

$$U_x = \frac{M}{2}U_{\text{dc}} = \frac{M}{2}\frac{1+D}{1-3D}U_{\text{in}}, x = \text{a, b, c} \tag{4}$$

From Eq. (4), the output voltage of the SL-ZSI is related to M and D, usually $M + D \leqslant 1$; Greater boosting capacity is generally obtained by increasing D, As can be seen from Eq. (2), when D is increased to boost the boost factor B, the capacitor voltage stress also increases, so the system requires capacitors with a higher voltage withstand capability. Moreover, the increase in D is accompanied by a decrease in M, which affects the output power quality of the system. In addition, when the SL-ZSI is in the straight-through state, the diode D_{in} cuts off, making the input current intermittent, reducing the utilisation of the DC source and affecting the service life of the DC source.

3. High gain modified switching inductive z-source inverter

The proposed high gain modified switched inductor Z-source inverter is shown in Fig. 3. This topology builds on the SL-ZSI by replacing the diode in the switched inductor with a capacitor, changing the order of connection of the components in its switched inductor module and combining to form two high boost units, which gives the impedance source network section a higher boost factor. The addition of an inductor and active switch behind the DC source, forming a BOOST circuit with the front stage, further improves the boosting capability and allows for less inrush current in the network at start-up, ensuring continuous input current and improving the utilisation of the DC source.

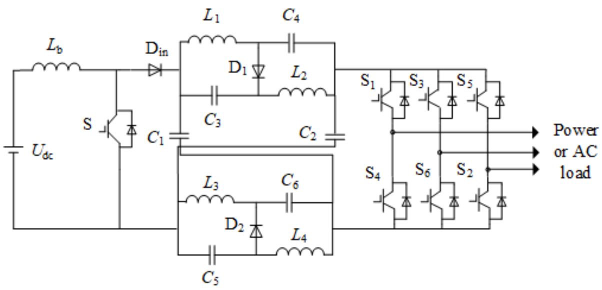


Fig. 3. HISL-ZSI topology

Fig. 4 shows two equivalent circuits for the high gain modified switched inductor Zsource inverter in both the straight-through and non-straight-through states.

When the HISL-ZSI is in the straight-through state, the equivalent circuit is shown in Fig. 4(a): as the load side is short-circuited, the inverter bridge can be replaced by a wire. Diodes D_{in}, D_1 and D_2 are cut off in reverse. Inductor L_b provides a continuity loop for the DC source in the HISL-ZSI straight-through state, so that the input current is continuous. DC source U_{dc} and capacitors C_1, C_3, C_4 and C_2, C_5 and C_6 charge inductor L_b as well as L_1, L_2 and L_3, L_4 respectively.

When the HISL-ZSI is in the non-pass-through state, the equivalent circuit is shown in Fig. 4(b): In the active state, the inverter bridge and the load can be equated to an ideal current source. In the conventional zero state, the inverter bridge and the load can be equated to a zero-value current source. When the system is in these two states, the diodes $D_{in,}$ D_1 and D_2 are in positive conduction and the DC source U_{in} and the inductors L_b, L_1, L_2, L_3 and L_4 supply the capacitors $C_1, C_2, C_3, C_4, C_5, C_6$ and the load.

Let $L_1 = L_2 = L_3 = L_4, C_1 = C_2, C_3 = C_4 = C_5 = C_6$. Then the impedance source network is symmetrical and yields:

$$\begin{cases} U_{L1} = U_{L2} = U_{L3} = U_{L4} \\ U_{C1} = U_{C2} \\ U_{C3} = U_{C4} = U_{C5} = U_{C6} \end{cases} \tag{5}$$

From the through state equivalent circuit in Fig. 4(a), it follows that :

$$\begin{cases} U_{in} = U_{L\,b} \\ U_{L1} = U_{C1} + U_{C4} \\ U_{dc} = 0 \end{cases} \tag{6}$$

From the non-through state equivalent circuit in Fig. 4(b), it follows that :

$$\begin{cases} U_{in} = U_{L\,b} + U_{C1} - U_{C6} - U_{C5} \\ U_{dc} = U_{C2} + U_{C5} + U_{C6} \\ U_{L1} = -U_{C3} \end{cases} \tag{7}$$

Let the switching period be T_s, the pass-through time be T_1 and the pass-through duty cycle be D_0. According to the volt-second balance principle, for inductor L_1 averaged over one switching period is 0 :

$$D_0 \left(U_{C1} + U_{C4}\right) - \left(1 - D_0\right) U_{C3} = 0 \tag{8}$$

The relationship between the voltages U_{C3} and U_{C1} across capacitor C_3 and C_1 can be obtained by simplifying Eq. (8) as:

$$U_{C1} = \frac{1 - 2D_0}{D_0} U_{C3} \tag{9}$$

Substituting Eq. (9) into Eq. (8)) gives:

$$\begin{cases} U_{in} = U_{L\,b} + \frac{1-4D_0}{D_0} U_{C3} \\ U_{dc} = \frac{1}{D_0} U_{C3} \end{cases} \tag{10}$$

Similarly, according to the volt-second balance principle, for an inductance L_b averaged over one switching cycle is 0 :

$$D_0 U_{in} + \left(1 - D_0\right) \left(U_{in} + \frac{4D_0 - 1}{D_0} U_{C3}\right) = 0 \tag{11}$$

Simplifying Eq. (11) yields:

$$U_{in} = \frac{\left(1 - 4D_0\right)\left(1 - D_0\right)}{D_0} U_{C3} \tag{12}$$

The relationship between the dc source U_{in} and the dc bus voltage U_{dc} can be obtained by combining Eqs. (10) and (12):

$$U_{dc} = \frac{1}{\left(1 - D_0\right)\left(1 - 4D_0\right)} U_{in} \tag{13}$$

In summary, it follows that:

$$\begin{cases} U_{C3} = U_{C4} = U_{C5} = U_{C6} = \frac{D_0}{(1-4D_0)(1-D_0)} U_{in} \\ U_{C1} = U_{C2} = \frac{1-2D_0}{(1-4D_0)(1-D_0)} U_{in} \\ U_{dc} = \frac{1}{(1-4D_0)(1-D_0)} U_{in} = BU_{in} \end{cases} \tag{14}$$

B in Eq. (14) is the boost factor of the HISL-ZSI topology.

If the modulation factor of the inverter is M, the peak output voltage of the inverter is:

$$U_x = \frac{M}{2} U_{dc} = \frac{M}{2\left(1 - 4D_0\right)\left(1 - D_0\right)} U_{in} = \frac{M}{2} BU_{in}, x = a, b, c \tag{15}$$

Typical Z-source inverter topologies are compared below for boost factors as shown in Table 1, Fig. 5.

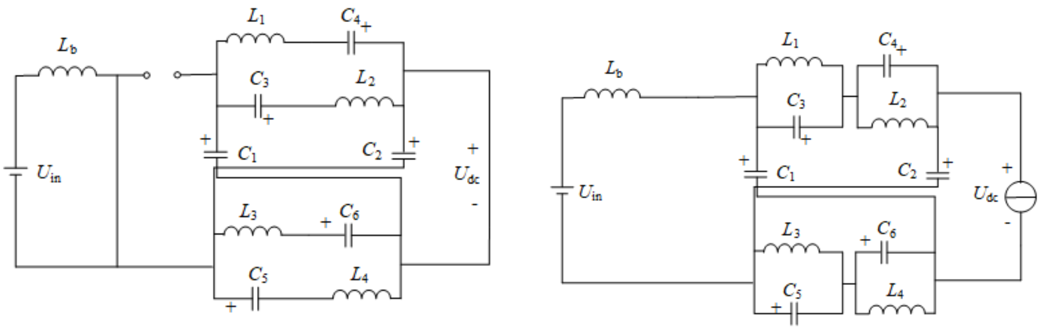
As can be seen in Fig. 5, the HISL-ZSI topology in this paper has a large improvement in boosting capability compared to several typical topologies. If the output voltage is the same, the HISL-ZSI topology can control D_0 to a smaller value and the modulation factor M is larger compared to other topologies, thus ensuring good output power quality.

Due to the addition of the pre-stage inductor L_b, as shown in Fig. 6, the current flowing through the inductor cannot change abruptly during startup, and the startup current is very small, and it will not happen that the capacitor voltage will be instantaneously charged to $0.5U_{in}$ and the inductor-capacitor in the circuit starts to resonate, so there is no need for a soft-start strategy.

Moreover, the inductor L_b shown by Fig. 7 provides a continuous current loop for the DC source U_{in} when the inverter is in the on-state, which improves the utilisation of the DC source.

4. Modulation strategy

There are four modulation strategies commonly used in ZSI, namely simple boost control, maximum boost control, third harmonic injection control, and straight-through segmented SVPWM control [27–29]. ZSI uses a straight through zero state to achieve the boost, but as the output state of the inverter is related to the effective state, in order not to affect the output state of the inverter, a straight through state is usually used to replace part of the traditional zero state [30, 31], thus achieving the purpose of generating a straight through to complete the boost without affecting the output state of the inverter [32–34]. This



(a) Equivalent circuit diagram of through state (b) Equivalent circuit diagram of non-through state

Fig. 4. HISL-ZSI equivalent circuit

Table 1. Typical ZSI booster factor

Z-source topology	Boosting factor B
Conventional Z-source inverters(ZSI)	$1/(1-2D)$
Enhanced Z-source inverters(E-ZSI)	$1/\left(1-4D+2D^2\right)$
Inverter with coupled inductive Z-source(I-ZSI)	$(1+4D)/\left(1-2D-4D^2\right)$
Parallel Z-source inverters(P-ZSI)	$1/(1-3D)$
New Z-source inverter(NEW ZSI)	$1/(1-2D)(1-D)$
Switching inductive Z-source	$(1+D)/(1-3D)$
inverters(SL-ZSI)	$1/(1-4D)(1-D)$
HISL-Z source inverter	$1/(1-4D)(1-D)$

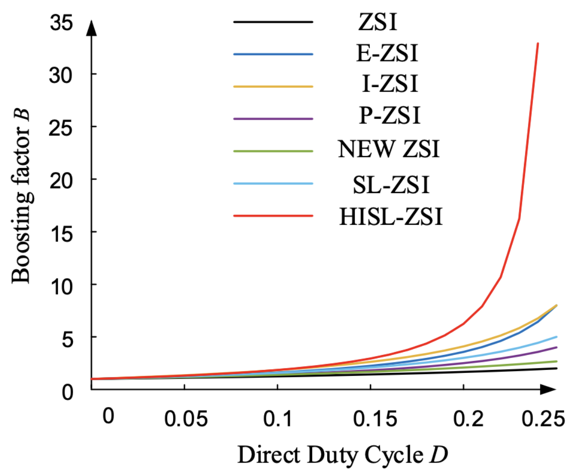


Fig. 5. Comparison of typical ZSI boost factors

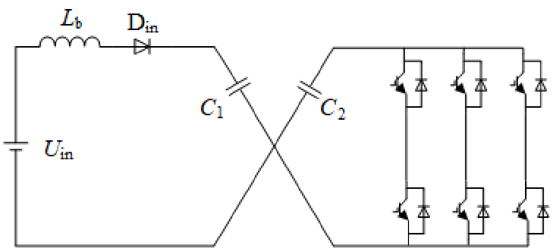


Fig. 6. HISL-ZSI equivalent circuit at start-up

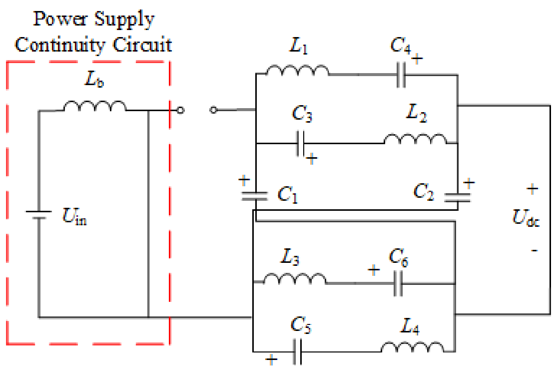


Fig. 7. Schematic diagram of HISL-ZSI Continuity Circuit

paper uses a simple boost control modulation strategy. The simple boost control principle is simple and easy to implement, and the switching tube current is small, so it is widely used.

The schematic diagram of the simple boost control method is shown in Fig. 8. The modulation strategy is based on SPWM with a constant delta carrier value V_p greater than the positive peak of the sine wave and a constant delta carrier value Vn less than the negative peak of the sine wave. When the delta carrier value in the modulation is greater than V_p or less than V_n, the three phase bridge arms of the inverter conduct simultaneously, thus creating a straightthrough state and ensuring that it is inserted in the conventional zero state.

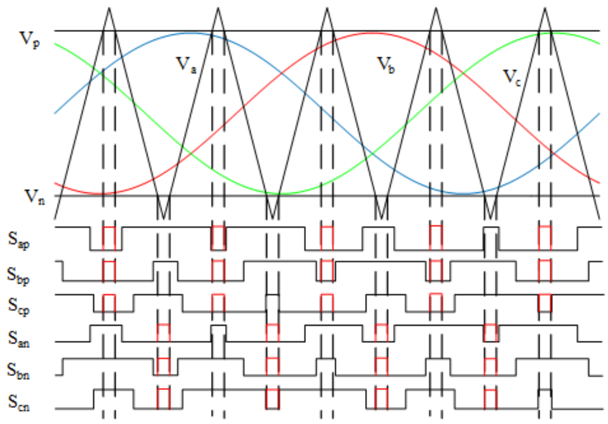


Fig. 8. Simple booster control schematic

From Fig. 8 it can be seen that the through duty cycle is:

$$D_0 = \frac{T_1}{T_s} = 1 - \frac{V_P}{V_t} \tag{16}$$

where T_s is the switching period, T_1 is the through time and V_t is the amplitude of the delta carrier.

Since $|V_p|, |V_n| \geq |V_x|, (x = a, b, c)$, the maximum value of the through duty cycle D_{max} is:

$$D_{max} = 1 - M \tag{17}$$

Coupling Eqs. (14) and (16) yields the peak output voltage of the inverter as:

$$U_{x\,max} = \frac{1}{2(4M-3)} U_{in}\,, x = a, b, c \tag{18}$$

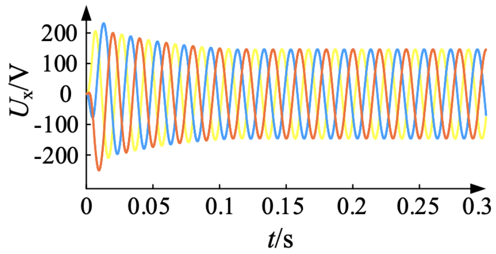
From Eq. (18) it can be seen that reducing the modulation factor M will increase the output voltage amplitude, but this will also increase the voltage stress on the power device and reduce the output power quality. This can make it impossible to meet the output AC voltage required for some applications due to the voltage rating of the device.

5. Simulation verification analysis

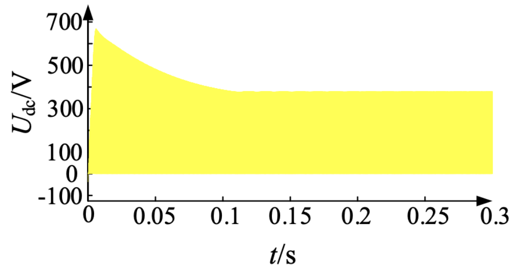
In order to verify the above theoretical analysis, the SL-ZSI topology and the HISL-ZSI type topology were modelled and simulated under simple boost control using Simulink software, with the following specific parameter settings for the HISL-ZSI topology: DC voltage sources: Z network inductors $L_1 = L_2 = L_3 = L_4 = 460$mH, Z network capacitors $C_1 = C_2 = 1000\mu$F, $C_3 = C_4 = C_5 = C_6 = 470\mu$F, Pre-stage inductors $L_b = 1$mH, Output filter inductors $L_f = 45$mH, Output filter capacitors $C_f = 30\mu$F, Carrier frequency $f_c = 10$kHz.

The simulation results for SL-ZSI and HISL-ZSI at an input voltage of 150 V are plotted in Figs. 9 and 10, respectively. With modulation factor $M = 0.8$ and through duty cycle $D_0 = 0.18$ set, As can be seen from Fig. 9 after the SL-ZSI system has stabilised, the SL-ZSI output voltage $U_x = 152$ V, the DC chain voltage $U_{dc} = 379$ V, and the capacitor voltage $U_{C1} = U_{C2} = 270$ V. As can be seen from Fig. 10, after the HISL-ZSI system is stabilised, the HISLZSI output voltage $U_x = 260$ V, the DC chain voltage $U_{dc} = 653$ V, the capacitor voltage $U_{C1} = U_{C2} = 418$ V, $U_{C3} = U_{C4} = U_{C5} = U_{C6} = 117$ V, and substituting $D_0 = 0.18$ into Eqs. (14) and (15) yields a theoretical value that agrees with the simulated output value, verifying The theoretical value is consistent with the simulated output, verifying its correctness. The total harmonic distortion rate (THD) of the output voltage is 0.19%, and the output voltage quality is good. By comparing Fig. 9 with Fig. 10, it can be seen that at system start-up, when the input voltage U_{in}, modulation ratio M and through duty cycle D_0 are the same, the boost factor B of the HISL-ZSI topology = 4.36, while the boost factor B of the SL-ZSI topology is only 1.56. The boost gain of the HISL-ZSI is higher, the output side load voltage is stable and the output voltage quality is high, but the capacitor voltage However, the capacitor voltage stress is correspondingly higher, requiring a larger capacitor withstand voltage capability, which needs further improvement.

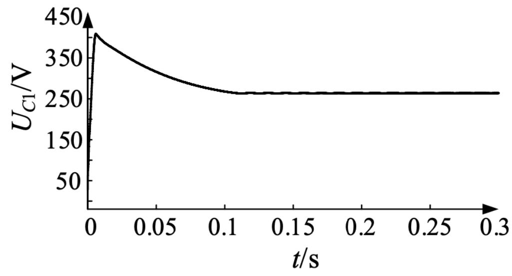
Fig. 11 shows the HISL-ZSI simulation results for an input voltage of $U_{in} = 150$ V and an output voltage of $U_x = 152$ V. As can be seen from Fig. 11, after the HISL-ZSI system has stabilised, the HISL-ZSI output voltage $U_x = 152$ V, the DC chain voltage $U_{dc} = 380$ V and the capacitor voltage $U_{C1} = U_{C2} = 260$ V. substituting $D_0 = 0.133$ and $M = 0.82$ into Eqs. (14) and (15) yields a theoretical value that agrees with the simulated output value, Comparing Fig. 9, it can be seen that the HISL-ZSI requires a through duty cycle of $D_0 = 0.133$ and $M = 0.82$ while keeping the input and output voltages the same, compared to the SL-ZSI it requires a smaller D_0 and a larger M. The capacitor therefore has a higher quality output voltage and reduced voltage stress. Therefore, if both topologies are to maintain the same, higher boost gain, the SL-ZSI topology will need to reduce the modulation factor M and increase the through duty cycle D_0, which will cause distortions in the output waveform, reducing power quality and with it higher capacitor voltage stress.



(a) Three-phase voltage



(b) DC chain voltage



(c) Capacitance voltage

Fig. 9. When $U_{\text{in}} = 150$ V, $D_0 = 0.18$: SL-ZSI topology simulation result diagram

6. Simulation verification analysis

In this paper, a high-gain modified switched-inductor Z-source inverter topology is proposed, which is compared with the switched-inductor inverter topology for steady-state principle analysis and simulation verification. The results show that

1. the HISL-ZSI topology has a high boost gain when the through duty cycle is small, but the capacitor voltage stress is correspondingly high, requiring a larger capacitor withstanding capacity, which needs further improvement;

2. Compared to the SL-ZSI, the HISL-ZSI requires only a smaller through duty cycle for the same voltage output under the same input conditions, allowing for a higher modulation factor to be maintained, reducing voltage stress on the switching device and improving output power quality;

3. The HISL-ZSI impedance source network has low capacitive voltage stress, which reduces the size of the capacitor and saves costs.

Thus, it can be used in new energy generation applications with low input voltage. In addition, the HISLZSI has the ability to maintain continuous input current and some suppression of start-up surges.

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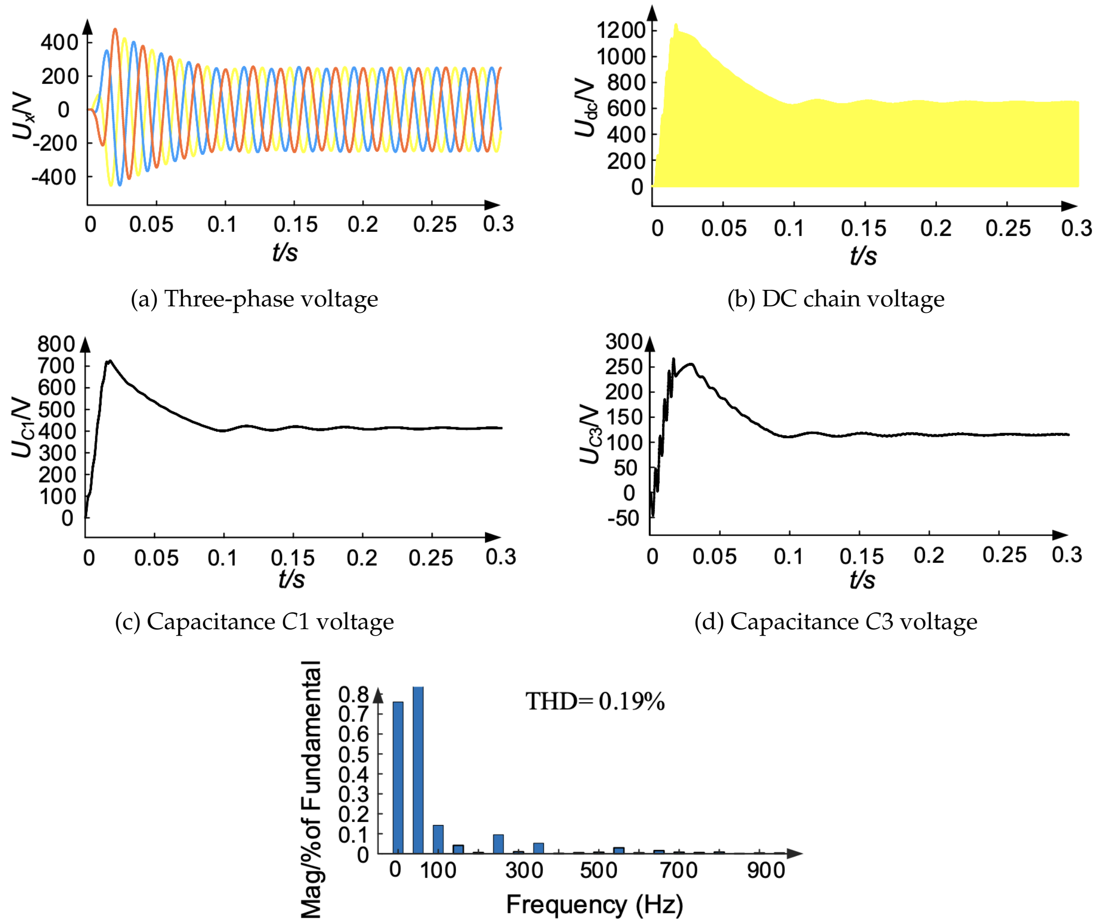

(a) Three-phase voltage

(b) DC chain voltage

(c) Capacitance $C1$ voltage

(d) Capacitance $C3$ voltage

(e) Harmonic distortion rate

Fig. 10. When $U_{\text{in}} = 150$ V, $D_0 = 0.18$: HISL-ZSI topology simulation result diagram

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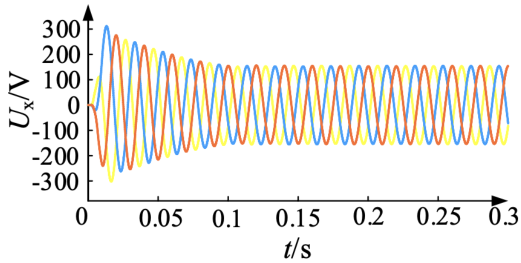
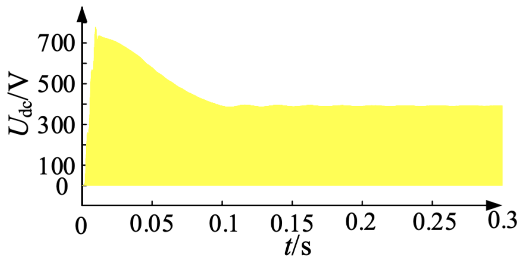
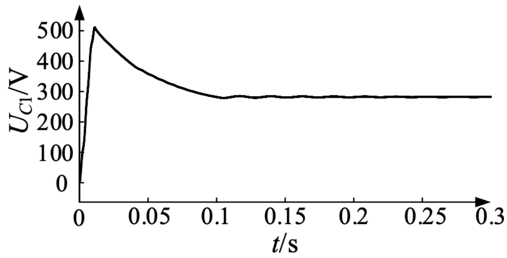


(a) Three-phase voltage



(b) DC chain voltage



(c) Capacitance $C1$ voltage

Fig. 11. When $U_{in} = 150$ V, $D_0 = 0.133$, $U_x = 152$ V : HISL-ZSI topology simulation result diagram

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