Linear Extended State Observer-Based Backstepping Sliding Mode Control For DC-Bus Voltage Regulation Under Constant Power Loads In DC Microgrids

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In DC microgrids, Constant Power Load (CPL) is one of the causes to generate negative incremental resistance, which significantly reduces the stability margin and may lead to DC-bus voltage fluctuations. Therefore, the issue of handling the DC-bus voltage under the CPL is of considerable interest. In this paper, a Linear Extended State Observer-based Backstepping Sliding Mode Control (LESO-BSMC) strategy is proposed to enhance the robustness of output voltage for a boost converter under CPL and system uncertainties. A two-channel Linear Extended State Observer (LESO) is designed to estimate real-time disturbances caused by load variations, input-voltage fluctuations, and parameter mismatches, allowing for accurate compensation without relying on a detailed nonlinear model. The Backstepping Sliding Mode Control (BSMC) law is constructed based on the Lyapunov stability criteria to guarantee global stability, fast dynamic response, and reduced control chattering. Comprehensive simulations were conducted to confirm the effectiveness of the proposed algorithm for maintaining DC-bus voltage at 24 V under four scenarios. The obtained results demonstrate that the proposed LESO-BSMC strategy achieves high tracking performance, efficiency in disturbance rejection and robustness, faster dynamic recovery, and minimizes DC-bus voltage ripple in comparison to other strategies of PI-SMC and Adaptive BSMC (ABSMC), while significantly reducing switching activity as quantified by control-effort indices.

Keywords: Constant Power Load, DC Microgrid, DC-Bus Voltage, Linear Extended State Observer, Sliding Mode Control.

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1. Introduction

Direct current microgrids (DCMGs) have attracted increasing attention due to their high transmission efficiency, low conversion losses, and flexibility in integrating renewable energy sources (RESs), storage units, and DC loads [1, 2]. The configuration of a typical DCMG is shown in Fig. 1 with the DC bus serving as the core node that links multiple subsystems, maintaining stable voltage and instantaneous power balance between sources and loads. However, guaranteeing the DC-bus voltage is facing challenges due to the nonlinear characteristics and uncertainties caused by input-voltage fluctuations, switching disturbances, parameter mismatches, and especially the effect of CPLs. In the DCMG system, CPLs are commonly generated by power electronic converters (DC-DC or DC-AC) to regulate con-

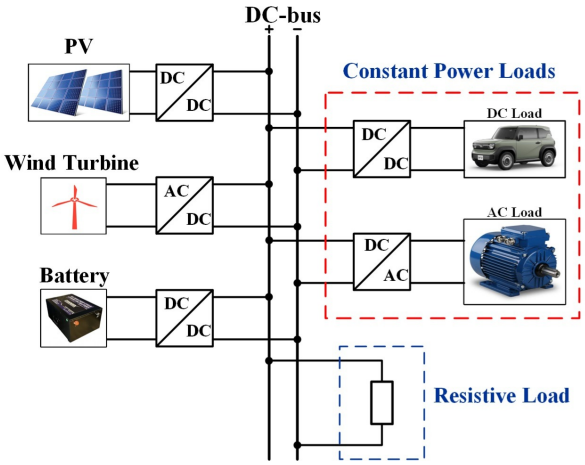

Fig. 1. A Typical DCMG Structure.

stant output power. When the DC-bus voltage decreases, the CPLs current rises to maintain constant power, thereby exhibiting a negative incremental impedance that deteriorates the system damping, reduces the stability margin, and may even cause severe DC-bus voltage oscillations [3–5].

To mitigate the adverse effects of CPLs, various control strategies have been investigated. For the conventional strategy, passive damping methods employing RLC components or passive filters were conducted to increase the damping ratio and suppress oscillations. However, these methods lead to higher power loss, increased hardware size, and are unsuitable for compact systems or high power-density converters [6]. Subsequently, active damping techniques were developed through current-feedback control, virtual impedance adjustment, or pole-shifting approaches to enhance voltage stability. Nevertheless, their effectiveness is mainly limited around the nominal operating point and degrades under large disturbances or strong nonlinear conditions [3, 7].

To achieve the voltage stability under significant dynamic variations, several nonlinear control schemes for DCMGs have been utilised. In [8], an Exact Feedback Linearization (EFL) technique was proposed to transforms nonlinear systems into equivalent linear ones, facilitating controller design using linear control theory. Nevertheless, EFL depends significantly on correct modelling and is sensitive to parameter variations and external disturbances [9–11]. Meanwhile, Sliding Mode Control (SMC) offers strong robustness and simple design, but it suffers from chattering and switching frequency limitations [12–16]. For the backstepping method, systematic design steps is applied to ensure global stability based on the Lyapunov stability criterion. However, its performance may deteriorate when the system model is inaccurate or subject to strong parameter uncertainty [17]. Furthermore, nonlinear control techniques were proposed [18, 19] to leverage their respective strengths and overcome individual drawbacks. Among these methods, the BSMC strategy [17, 20, 21] is known as an advanced technique that has attracted a lot of interest as an effective solution for enhancing system robustness and dynamic performance. In [22], Wu et al. developed an ABSMC for DC-DC converters feeding CPLs, where adaptive tuning was used to maintain voltage stability under load and input variations. However, the performance of ABSMC still depends strongly on model accuracy and adaptive parameter selection, while unmodeled dynamics and fast disturbances are not fully compensated. Besides, Model Predictive Control (MPC) [23–25] enables real-time optimization and constraint handling but requires high computational effort, making it less feasible for fast-switching converters.

Recently, observer-based control schemes have been adopted to enhance disturbance rejection in DCMGs. In LESO-SMC strategies [18, 26–28], a LESO estimates a lumped total disturbance that is compensated within the SMC framework. Although these methods provide robustness against matched and mismatched uncertainties, the disturbance is typically represented as a single aggregated term in the original state coordinates, without explicitly separating the internal power flow dynamics associated with CPLs. Meanwhile, ObserverBased Backstepping (OBB) approaches [29–31] improve disturbance rejection through realtime estimation and feedforward compensation of lumped uncertainties. Although global stability can be ensured via Lyapunov-based design, robustness largely depends on observer accuracy and gain tuning. Unlike sliding-mode-based structures, an explicit invariant error manifold is not established, and resilience to severe nonlinear CPL-induced effects relies primarily on estimation performance rather than structural invariance.

Motivated by the aforementioned shortcomings, this paper proposes a structured LESO-BSMC strategy for DC-bus voltage stabilization of DC-DC boost converters supplying CPLs. The primary contributions are highlighted as follows. First, compared with LESO-SMC approaches [18, 26–28], which estimate lumped disturbances directly in the original state coordinates, the proposed method employs an energy-based exact feedback linearization to transform the boost converter with CPL into a Brunovsky-type canonical form. This reformulation explicitly structures the internal power-flow dynamics, providing a systematic basis for the development of a dual-channel LESO and facilitating a structured treatment of the non-minimum phase

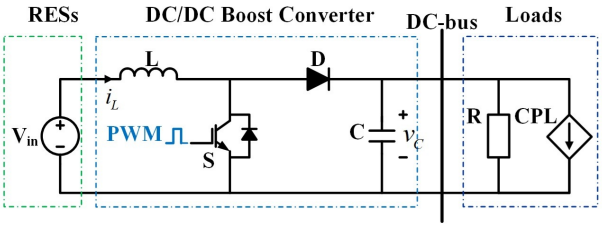

Fig. 2. The Simplified DC Distribution System.

behavior associated with direct output selection. Second, in contrast to OBB methods [29–31], where robustness is typically achieved through disturbance estimation accuracy and gain tuning, the proposed framework integrates an integral-augmented sliding surface into the observer-backstepping structure, enhancing disturbance rejection capability while strengthening robustness through integral error dynamics. Third, unlike ABSMC [22], which attains robustness through adaptive parameter updating, the proposed strategy achieves disturbance attenuation via real-time reconstruction using LESO, enabling direct compensation of model uncertainties and input-voltage variations. Finally, a unified LESO - BSMC framework is developed, ensuring Lyapunov-based global stability while mitigating chattering through disturbance reconstruction combined with an integral-augmented sliding surface.

The rest of this paper is organized as follows. Section 2 describes the materials and methods of the proposed LESO-BSMC strategy. Section 3 presents and discusses the simulation results under various operating conditions. Section 4 concludes the paper.

2. Materials and methods

2.1. System Modelling

Consider a simplified DC distribution system is shown in Fig. 2. In this configuration, the DC-bus serves as the core node that interconnects distributed energy sources through a boost converter and supplies power to both the resistive load (R) and the constant power load (CPL) connected in parallel to the DC-bus. The CPL is modelled as a load that maintains a constant consumed power P_{CPL}, which introduces a negative incremental impedance characteristic and significantly reduces voltage damping.

Assumption 1: The boost converter operates in Continuous Current Mode (CCM), with switching losses and parasitic resistances neglected. The capacitor voltage remains strictly positive, $v_C > 0$, ensuring a well-defined CPL term P_{CPL}/v_C.

Under Assumption 1, the averaged state-space model can be obtained by analyzing the converter dynamics in the

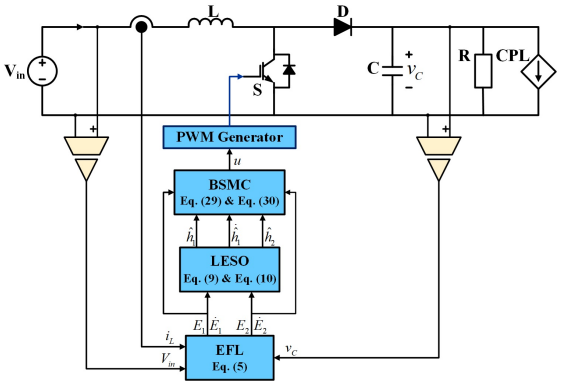

Fig. 3. Block diagram of the proposed LESO-BSMC control strategy.

ON and OFF switching states of switch S . The nonlinear averaged model is derived as:

$$\begin{cases} \dot{i}_L = -\frac{(1-u)}{L} v_C + \frac{V_{in}}{L} \\ \dot{v}_C = \frac{(1-u)}{C} i_L - \frac{v_C}{RC} - \frac{P_{CPL}}{v_C} \end{cases} \tag{1}$$

where i_L is the inductor current, v_C is the capacitor voltage, V_{in} is the input voltage, and $u \in [0,1]$. The term P_{CPL}/v_C reflects the negative incremental impedance effect of CPLs, resulting in a highly nonlinear and inadequately damped system.

2.2. Block Diagram of the Proposed Control Strategy

Fig. 3 illustrates the overall structure of the proposed LESO-BSMC scheme for the boost converter supplying a composite load consisting of a resistor in parallel with a CPL. The inductor current i_L, capacitor voltage v_C and input voltage V_{in} are measured and used as feedback signals. First, an energy-based exact feedback linearization (EFL) block maps the original states into the energy-coordinate variables (E_1, E_2), providing a structured representation for subsequent controller synthesis. Then, a dual-channel LESO reconstructs the lumped uncertainties and disturbances in the transformed dynamics, denoted by $\hat{h}_1, \dot{\hat{h}}_1, \hat{h}_2$. Based on (E_1, E_2) and the estimated disturbances, the backstepping sliding-mode controller generates the continuous control signal u, which is implemented through a PWM generator to drive the switching device S . The detailed derivations of the EFL transformation, LESO design, and the LESO-compensated BSMC law are presented in Sections 2.3-2.5, respectively.

2.3. Energy-based Exact Feedback Linearization

To design the proposed control strategy, the nonlinear averaged model in Eq. (1) is first examined using an energy-based EFL framework. A direct selection of the inductor

current or the capacitor voltage as the output leads only to partial feedback linearization, which fails to ensure well-behaved zero dynamics, especially under the destabilizing negative incremental impedance of CPLs. Such selections typically yield weakly damped internal dynamics and degraded voltage regulation performance. Therefore, a generalized output function derived from the stored electromagnetic energy is considered to achieve fully linearizable system dynamics and guarantee inherent stability [22].

The energy-based virtual output is defined as:

$$E(x) = \frac{1}{2}Li_L^2 + \frac{1}{2}Cv_C^2 \tag{2}$$

Taking the time derivative gives the power balance associated with the stored energy as follows:

$$\dot{E} = V_{in}i_L - \frac{v_C^2}{R} - P_{CPL} \tag{3}$$

This energy relation highlights how the CPL term enters the system dynamics and alters the internal power balance. Motivated by this observation, the physical state vector $x = [i_L, v_C]^T$ is mapped into an energy-based coordinate representation that provides a more structured basis for controller synthesis. The transformed coordinate is described by [32]:

$$\begin{cases} E_1 = \frac{1}{2}Li_L^2 + \frac{1}{2}Cv_C^2 \\ E_2 = V_{in}i_L - \frac{v_C^2}{R_n} \end{cases} \tag{4}$$

where E_1 represents the stored electromagnetic energy, directly associated with the DC-bus voltage regulation objective; E_2 characterizes the nominal power balance between the source and the composite load modeled by its nominal equivalent resistance R_n. Deviations from this nominal model, including parameter uncertainties, CPL negative impedance effects, and unmodeled converter dynamics, are grouped into disturbance terms.

Differentiating Eq. (4) results in the Brunovsky-type canonical form is calculated as:

$$\begin{cases} \dot{E}_1 = E_2 + h_1 \\ \dot{E}_2 = d + h_2 \end{cases} \tag{5}$$

in which

$$d = \frac{V_{in}^2}{L} + \frac{2v_C^2}{CR_n^2} - \left(\frac{V_{in}v_C}{L} + \frac{2i_Lv_C}{CR_n}\right)(1-u) \tag{6}$$

$$h_1 = \frac{v_C^2}{R_n} - \frac{v_C^2}{R} - P_{CPL} \tag{7}$$

$$h_2 = -\frac{2}{CR_n}\left(\frac{v_C^2}{R_n} - \frac{v_C^2}{R} - P_{CPL}\right) \tag{8}$$

where h_1 represents the aggregated disturbance capturing power mismatch between the nominal load model and the actual composite load including the CPL; h_2 represents the corresponding disturbance in the power-balance channel propagated through the energycoordinate dynamics; d is the auxiliary variable.

Moreover, any bounded variation in the input voltage V_{in} is regarded as part of the lumped disturbance and absorbed into h_1 and h_2, without altering the relative degree or the canonical feedback linearization structure.

Assumption 2: The lumped disturbance functions $h_i(t), i = 1,2$, are bounded and piecewise continuously differentiable. There exist positive constants $\bar{h}_i$ and $\bar{\rho}_i$ such that: $|h_i(t)| \le \bar{h}_i$, $|\dot{h}_i(t)| \le \bar{\rho}_i$.

Remark 1: Assumption 2 is standard in ESO design [33], where the lumped disturbance is assumed to be bounded to guarantee bounded estimation error dynamics. In practical DCMGs, disturbances arising from CPL power variations and input-voltage fluctuations are physically bounded and governed by converter and load dynamics, thereby satisfying this condition.

The transformation in Eq. (4) - Eq. (8) fully linearizes the internal dynamics, enabling independent shaping of the tracking error dynamics and facilitating disturbance estimation via the LESO. This energy-coordinate representation establishes a well-conditioned foundation for developing the subsequent BSMC controller.

2.4. LESO Design

Based on the canonical energy-coordinate model in Eq. (5), the lumped disturbances h_1, h_2 can be regarded as extended states that need to be estimated. Therefore, a dual-channel LESO is constructed as follows [33, 34]:

$$\text{LESO-1:} \begin{cases} \dot{\hat{E}}_1 = \hat{E}_2 + \hat{h}_1 + L_{11}\left(E_1 - \hat{E}_1\right) \\ \dot{\hat{h}}_1 = L_{12}\left(E_1 - \hat{E}_1\right) \end{cases} \tag{9}$$

$$\text{LESO-2:} \begin{cases} \dot{\hat{E}}_2 = d + \hat{h}_2 + L_{21}\left(E_2 - \hat{E}_2\right) \\ \dot{\hat{h}}_2 = L_{22}\left(E_2 - \hat{E}_2\right) \end{cases} \tag{10}$$

where $\hat{E}_1, \hat{E}_2$ are the estimated transformed states, and $\hat{h}_1, \hat{h}_2$ are the estimated disturbances.

From a physical standpoint, the first observer channel reconstructs the energy-rate mismatch h_1, which arises from practical disturbances in DCMGs such as CPL-induced power fluctuations and load uncertainties, while the second channel captures its propagation into the power-balance dynamics. As shown in Eq. (7) - Eq. (8), h_2 is proportional to h_1 confirming that the second channel does not represent an independent disturbance source. This dualchannel

structure enables physically consistent disturbance reconstruction for the subsequent backstepping sliding-mode controller.

The observer gains are selected according to the standard bandwidth-based rule [35, 36]:

$$\begin{bmatrix} L_{i1} \\ L_{i2} \end{bmatrix} = \begin{bmatrix} 2\omega_{0i} \\ 2\omega_{0i}^2 \end{bmatrix}, \quad \omega_{0i} > 0, \quad i = 1, 2 \tag{11}$$

where ω_{0i} denotes the LESO bandwidth.

The observer gains are tuned using the bandwidth-parameterization principle, with observer poles placed at $-\omega_{0i}$, the observer bandwidth is selected as $\omega_{0i} \approx 5 - 10\omega_c$ to ensure sufficiently fast disturbance estimation, where ω_c denotes the closed-loop control bandwidth. Since the two channels correspond to different layers of the canonical energy-coordinate dynamics in Eq. (5), their bandwidths are tuned independently within this range. In particular, the second channel is assigned a higher bandwidth $(\omega_{02} > \omega_{01})$ to capture rapid power-balance variations, whereas the first channel is tuned more conservatively to reduce noise amplification. The final values are chosen as the largest admissible ones preserving closed-loop stability.

To assess convergence, the estimation errors can be defined as:

$$e_{i1} = E_i - \hat{E}_i, \quad e_{i2} = h_i - \hat{h}_i \tag{12}$$

The lumped error vector can be then obtained:

$$e_i = \begin{bmatrix} e_{i1} \\ e_{i2} \end{bmatrix} \tag{13}$$

Using Eq. (9) - Eq. (13), the estimation-error dynamics of each LESO channel are derived in compact form, and the corresponding characteristic polynomial shows that the homogeneous error system is exponentially stable for $\omega_{0i} > 0$. For time-varying but bounded disturbances satisfying Assumption 2, the error dynamics are Input-to-State Stable (ISS), and the steadystate estimation error can be made arbitrarily small by increasing the observer bandwidth ω_{0i}. The detailed proofs are provided in Appendix A. This property guarantees robust disturbance reconstruction, which is essential for the subsequent BSMC design.

2.5. LESO-Compensated Control Law

To enhance the robustness and disturbance rejection capability, the SMC law is integrated into a backstepping framework, where an LESO provides real-time estimation of the lumped disturbances.

The core idea is to decompose the nonlinear energy-based model into two cascaded subsystems and construct Lyapunov functions layer-by-layer, while the sliding mode term introduced in the final step strengthens robustness against uncertainties and improves tracking.

First, the primary tracking error is given by:

$$e_1 = E_1 - E_1^* \tag{14}$$

where the desired reference energy is chosen as:

$$E_1^* = \frac{1}{2} L i_{Ld}^2 + \frac{1}{2} C v_{Cd}^2 \tag{15}$$

with i_{Ld} and v_{Cd} denoting the desired inductor current and output capacitor voltage, respectively.

The first-layer Lyapunov function is selected as follows:

$$V_1 = \frac{1}{2} e_1^2 \tag{16}$$

Using the transformed dynamic in Eq. (5), the derivative of Eq. (14) is given by:

$$\dot{e}_1 = \dot{E}_1 - \dot{E}_1^* = E_2 + h_1 - \dot{E}_1^* \tag{17}$$

which leads to,

$$\dot{V}_1 = e_1 \left(E_2 + h_1 - \dot{E}_1^* \right) \tag{18}$$

To stabilize the first-layer error, the virtual control input is selected as:

$$E_2^* = -K_1 e_1 - \hat{h}_1 + \dot{E}_1^*, \quad K_1 > 0 \tag{19}$$

The second-layer error is defined as:

$$e_2 = E_2 - E_2^* \tag{20}$$

whose derivative is obtained using Eq. (5):

$$\dot{e}_2 = d + h_2 - \dot{E}_2^* \tag{21}$$

Substituting Eq. (19) - Eq. (21) into Eq. (17) yields the error relation:

$$\dot{e}_1 = e_2 - K_1 e_1 + \tilde{h}_1, \quad \tilde{h}_1 = h_1 - \hat{h}_1 \tag{22}$$

Consequently:

$$\dot{V}_1 = -K_1 e_1^2 + e_1 e_2 + e_1 \tilde{h}_1 \tag{23}$$

To enforce robust convergence of the second-layer dynamics, the augmented sliding surface is described as:

$$\sigma = e_2 + \lambda_1 e_1 + \lambda_2 \int_0^t e_1(\tau)\, d\tau, \quad \lambda_1 > 0, \lambda_2 > 0 \tag{24}$$

Taking the derivative of sliding surface Eq. (24) and using equations of Eq. (19), Eq. (21) and Eq. (22), the obtained equation is achieved as follows:

$$\dot{\sigma} = (\lambda_1 + K_1)\left(e_2 - K_1 e_1 + \tilde{h}_1\right) + \dot{\hat{h}}_1 - \ddot{E}_1^* + d + h_2 + \lambda_2 e_1 \tag{25}$$

Next, the composite Lyapunov function is considered as:

$$V_2 = V_1 + \frac{1}{2}\sigma^2 \tag{26}$$

Taking the derivative of the above Lyapunov function yields:

$$\dot{V}_2 = -K_1 e_1^2 + e_1 e_2 + e_1 \tilde{h}_1 + \sigma\dot{\sigma} \tag{27}$$

To make the sliding surface attractive and invariant, reaching law can be obtained as follows:

$$\dot{\sigma} = -K_2\sigma - K_S \text{sat}\left(\frac{\sigma}{\phi}\right), \quad K_2 > 0, K_S > 0, \phi > 0 \tag{28}$$

where $\text{sat}(\sigma/\phi)$ is the standard saturation function with boundary layer ϕ.

The auxiliary control input is achieved from Eq. (25) and Eq. (28) as follows:

$$\begin{aligned} d = & -(\lambda_1 + K_1)(e_2 - K_1 e_1) - \dot{\hat{h}}_1 + \ddot{E}_1^* \\ & - \hat{h}_2 - \lambda_2 e_1 - K_2\sigma - K_S \text{sat}\left(\frac{\sigma}{\phi}\right) \end{aligned} \tag{29}$$

Using Eq. (29) and the expression Eq. (6), the final control input is derived as:

$$u = 1 - \frac{\frac{V_{in}^2}{L} + \frac{2v_C^2}{CR_n^2} - d}{\frac{V_{in}v_C}{L} + \frac{2i_L v_C}{CR_n}} \tag{30}$$

Substituting Eq. (28) into Eq. (27) yields the derivative of the composite Lyapunov function.

Under appropriate gain selection as specified above, the closed-loop system satisfies a negative definite condition. Hence, the system is globally asymptotically stable when the disturbance estimation error vanishes, and input-to-state stable with respect to bounded observer errors. The detailed Lyapunov-based proof is provided in Appendix B. This guarantees robust voltage regulation and effective disturbance rejection even under rapid variations of the input voltage and CPL demand.

Remark 2: The proposed LESO-BSMC control strategy mitigates chattering through two coordinated mechanisms: (i) real-time disturbance reconstruction via the dual-channel LESO, which reduces the required switching gain K_S in Eq. (28), and (ii) the augmented sliding surface combined with a saturation function, which smooths the control action near the sliding manifold. Consequently, the reduction in control effort and switching activity will be quantitatively demonstrated in Section 3.

3. Results and discussion

To verify the effectiveness and robustness of the proposed control strategy, comprehensive simulations are implemented on the boost converter model in the MATLAB/Simulink environment. The system is evaluated under an input voltage of $V_{\text{in}} = 15$ V, with a desired DC-bus voltage of $v_{\text{Cd}} = 24$ V. The component parameters are selected as L $= 15\ \mu$H, C $= 1410\ \mu$F, R $= 15\ \Omega$, $\text{P}_{\text{CPL}} = 50$ W and a switching frequency of $f_{\text{SW}} = 50$ kHz.

In this study, the proposed LESO-BSMC controller is compared to two control strategies of PI-SMC and AB-SMC [22]. All controllers are implemented under identical operating conditions, including the same switching frequency and fixed-step discrete-time sampling period $T_S = 2 \times 10^{-6}$ s, with ode4 (Runge Kutta) solver. The LESO bandwidths ω_{01} and ω_{02} are selected according to the bandwidth-parametrization principle detailed in Section 2.4, ensuring sufficient disturbance estimation speed while preserving closed-loop stability. For a fair and consistent comparison, parameter tuning is conducted to ensure comparable voltage regulation accuracy, transient performance (e.g., settling time and overshoot) and output voltage ripple under the same test scenarios. This unified tuning criterion avoids performance bias toward any specific control method. The final parameter sets adopted in the simulations are summarized in Table 1. Besides, four simulation scenarios to evaluate the effectiveness of the proposed startegy that include variation of the input voltage V_{in} , variation of the CPL with and without parallel damping resistor R , and simultaneous variations of the input voltage and the CPL. To quantitatively evaluate regulation and control performance, four metrics are considered. The Root Mean Square Error (RMSE) and Integral of Absolute Error (IAE) are used to assess voltage regulation accuracy, while the Total Variation of the duty ratio (TVu) [37–39] is employed to evaluate control effort. The Root Mean Square of duty increments $(\text{RMS}(\Delta u))$ is additionally computed to quantify the average magnitude of duty-cycle fluctuations under fixed-frequency PWM operation. All metrics are calculated over the simulation interval $t \in [1.4, 1.6]$s to ensure consistent comparison.

Remark 3: The controller parameters in Table 1 were determined under the nominal operating condition ($V_{\text{in}} = 15$ V, $R = 15\Omega \| P_{\text{CPL}} = 50$ W) to meet unified transient targets. All controller gains were selected within the Lyapunov-admissible stability region to ensure closed-loop stability and consistency across controllers, with the

Table 1. Controller Parameters.

Controller	Parameters
PI-SMC	$K_P = 5.5, K_I = 2000, K_S = 0.9, \lambda = 18, \phi = 1.1$
ABSMC	$C_1 = 6 \times 10^3, K_2 = 2 \times 10^3, \varepsilon = 8 \times 10^5, \phi = 0.9$
LESO-BSMC	$\omega_{01} = 10\pi \times 10^3, \omega_{02} = 100\pi \times 10^3$ $K_1 = 9.5 \times 10^3, K_2 = 750, K_S = 4 \times 10^5 \lambda_1 = 2.4 \times 10^3,$ $\lambda_2 = 2 \times 10^3, \phi = 0.04$

PI and LESO parameters additionally tuned according to bandwidth-based tuning rules.

3.1. Case Study 1: Input Voltage Variation

Figure 4 illustrates the DC-bus voltage responses of the three controllers under step changes of the input voltage, with the load composed of a 50 W CPL connected in parallel with a 15Ω resistor.

When the input voltage drops abruptly from 18 V to 13 V at t = 1.6 s, significantly below the nominal operating point, the PI-SMC exhibits a voltage decrease of about 0.35 V , followed by a relatively slow recovery with noticeable oscillatory behavior, revealing an underdamped transient characteristic. The ABSMC reduces the undershoot and shortens the recovery time, maintaining the DC-bus voltage closer to 24 V with smaller ripple (less than 2%). In contrast, the proposed LESO-BSMC demonstrates the most robust behavior, keeping the DC-bus voltage nearly constant (deviation 0.1 V , ripple $< 0.5\%$) and recovering rapidly to steady state, indicating strong disturbance rejection capability.

A similar trend is observed when the input voltage increases from 13 V to 19 V at t = 1.7 s. The PI-SMC produces the largest overshoot of approximately 0.41 V , accompanied by a slower damping process compared with the other controllers. The ABSMC yields a smoother response, although ripple is still noticeable, around 0.25 V . Meanwhile, the proposed LESO-BSMC continues to achieve a fast and well-damped response, restoring the DC-bus voltage to 24 V with minimal deviation.

To further substantiate the observations from Fig. 4, Table 2 provides the quantitative error indices. The proposed LESO-BSMC reduces the RMSE by approximately 63% compared with PI-SMC and 80% compared with ABSMC. A similar improvement trend is observed in the IAE metric, confirming enhanced voltage regulation accuracy. More importantly, the control effort indicators clearly demonstrate significant chattering mitigation. The total variation of the control input (TVu) is reduced by more than 75%, and the RMS(Δu) decreases by nearly 4.5 times compared with both PI-SMC and ABSMC. This indicates substantially smoother control action and reduced switching activity. This reduction directly reflects effective suppression of high-frequency sliding-mode oscillations under fixed-frequency PWM implementation.

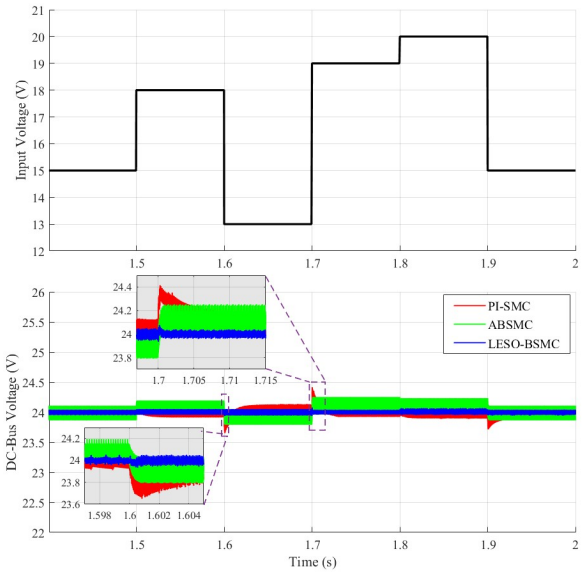

Fig. 4. Input Voltage Variation and DC-bus Voltage Responses.

Overall, the results confirm that the proposed LESO-BSMC achieves superior voltage regulation under large input voltage disturbances. By effectively compensating lumped disturbances, it improves stability, transient damping, and ripple suppression. The marked reductions in TVu and RMS(Δu) further verify significant chattering mitigation and smoother PWM control compared with PI-SMC and ABSMC in this case.

3.2. Case Study 2: CPL Variation with Parallel Resistor

Fig. 5 depicts the behavior of the DC-bus voltage when the CPL experiences abrupt changes while the input voltage remains fixed at 15 V and R = 15Ω is connected in parallel with the CPL. The two most critical instants occur at t = 1.6 s and t = 1.8 s, where the load conditions shift dramatically.

Table 2. Tracking and Control Effort Indices in Case Study 1

	RMSE	IAE	TVu	RMS($\Delta\mathbf{u}$)
PI-SMC	8.68×10^{-5}	5.324×10^{-8}	1.503×10^{4}	0.6297
ABSMC	16.48×10^{-5}	11.89×10^{-8}	1.328×10^{4}	0.6417
LESO-BSMC	3.236×10^{-5}	2.329×10^{-8}	3.632×10^{3}	0.1438

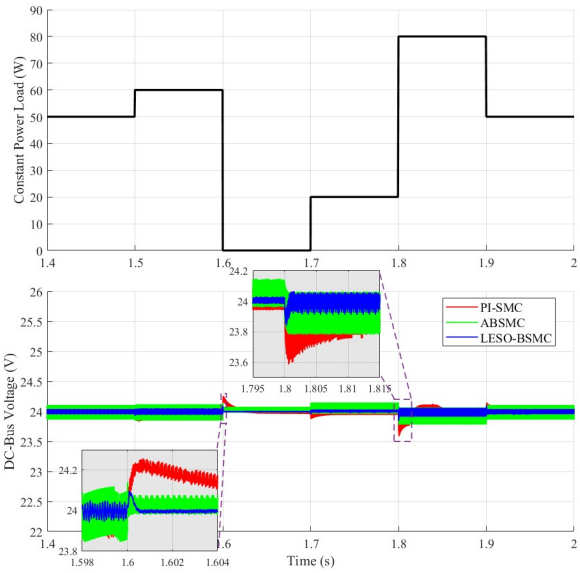

Fig. 5. CPL Variation and DC-bus Voltage Responses.

At t = 1.6 s, the CPL is suddenly removed, dropping from 60 W to 0 W . This unloading event causes the DC-bus voltage under the PI-SMC to peak at approximately 24.26 V , corresponding to an overshoot of about 0.26 V . The response is followed by pronounced oscillatory behavior with a sawtooth-like pattern, requiring nearly 0.02 s to decay before reaching steady state. The ABSMC produces almost no overshoot but maintains a ripple of about 0.1 V for a longer duration. In contrast, the proposed LESO-BSMC keeps the DC-bus voltage tightly regulated around the nominal 24 V , with a very small ripple of roughly 0.02 V , and achieves the fastest settling among the three controllers.

A different challenge appears at t = 1.8 s, when the CPL jumps sharply from 20 W to 80 W . This sudden increase in load results in a voltage drop on the DC-bus. The PI-SMC shows the largest sag, with the voltage dipping to approximately 23.58 V . The subsequent recovery is relatively slow and accompanied by sustained oscillations, indicating limited damping capability under severe load variation. The ABSMC responds with a smaller undershoot of about 23.8 V ; however, over the interval from 1.8 s to 1.9 s , the voltage oscillates between roughly 23.8 V and 24.06 V , indicating a larger ripple and a prolonged transient. The proposed LESO-BSMC once again demonstrates superior resilience: it exhibits only a shallow voltage dip, reaching a minimum of about 23.84 V and stabilizing within a very short interval. After the transient, the voltage remains confined within a narrow ripple band of approximately 23.91 V to 24.05 V , noticeably smaller than that of the other controllers.

Table 3 further confirms the robustness of the proposed strategy under abrupt CPL variations. While PI-SMC achieves lower tracking errors than ABSMC (approximately 26% lower RMSE and 35% lower IAE), this improvement comes at the expense of increased control activity, as reflected by about 15% higher TVu and 1.5% higher RMS(Δu). ABSMC slightly alleviates switching effort but accumulates larger regulation errors due to sustained oscillations during high-power transitions. In contrast, the proposed LESO-BSMC simultaneously attains the smallest error indices (RMSE $= 3.245 \times 10^{-5}$ and IAE $= 2.115 \times 10^{-8}$) and the lowest control-effort measures (Tvu $= 3.601 \times 10^{3}$ and RMS(Δu) $= 0.1479$), demonstrating improved disturbance compensation and enhanced stability under nonlinear load dynamics.

In Case Study 2, the parallel resistor mitigates the CPL's negative-impedance effect, leading to milder load disturbances. Despite this partial damping, the proposed LESO-BSMC still achieves the smallest voltage deviations, the fastest recovery, and the lowest oscillation level among the three controllers. This confirms its superior tracking and disturbance attenuation capability during abrupt CPL transitions, white also maintaining the lowest TVu and RMS(Δu), reflecting reduced switching activity and smoother control action.

3.3. Case Study 3: CPL Variation without Parallel Resistor

This is the most demanding case study, in which the DC-bus voltage is evaluated under variations of a pure CPL while the parallel damping resistor is removed. As depicted in Fig. 6, this condition fully exposes the negative-impedance effect of the CPL, greatly increasing the system's sensitivity to disturbances and oscillations, whereas the input voltage is kept constant at 15 V for all controllers.

When the CPL increases from 50 W to 80 W at t = 1.6 s, a severe transient is excited on the DC bus. The PI-SMC produces a noticeable deviation from the 24 V reference,

Table 3. Tracking and Control Effort Indices in Case Study 2

	RMSE	IAE	TVu	RMS($\Delta\mathbf{u}$)
PI-SMC	8.21×10^{-5}	5.001×10^{-8}	1.758×10^{4}	0.6992
ABSMC	11.14×10^{-5}	7.685×10^{-8}	1.532×10^{4}	0.6886
LESO-BSMC	3.245×10^{-5}	2.115×10^{-8}	3.601×10^{3}	0.1479

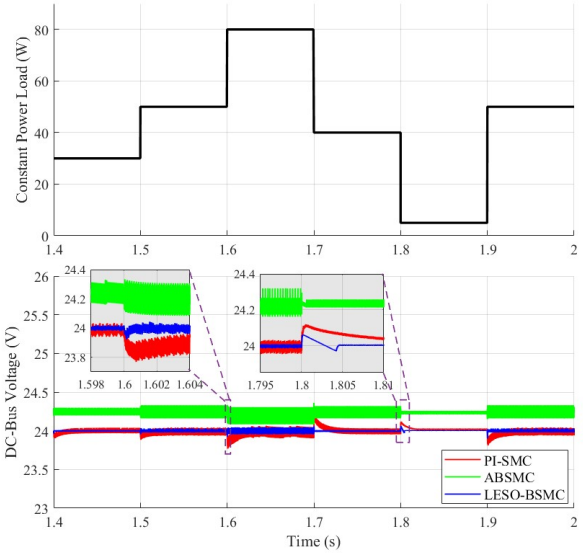

Fig. 6. CPL Variation and DC-bus Voltage Responses.

whereas the ABSMC exhibits the largest peak and pronounced wide band oscillations around the new operating point near 24.2 V , confirming that its sliding dynamics are strongly affected by the pure CPL. In comparison, the proposed LESO-BSMC exhibits only a very small undershoot of about 23.92 V and maintains the voltage excursion within a narrow ripple band of roughly 0.08 V. It then quickly returns to the 24 V operating level, demonstrating superior robustness against this heavy-load transition.

A more critical situation occurs at t $=$ 1.8 s, when the CPL abruptly drops from 40 W to 5 W. The PI-SMC-controlled DC-bus voltage settles within approximately 0.015 s and remains tightly regulated around 24.02 V , indicating a well-damped response under this unloading event. The ABSMC remains stable and moves to a new operating point around 24.25 V without noticeable overshoot, maintaining this shifted level throughout the load step with only a very small ripple of about 5 mV . In contrast, the proposed LESO-BSMC experiences a very short transient of about 4 ms with a small overshoot, after which the DC-bus voltage quickly returns to and stays close to the 24 V reference with the smallest ripple among the three controllers, showing a clear advantage in both tracking and disturbance attenuation.

As summarized in Table 4, removing the parallel damping resistor significantly enlarges the performance gap among the controllers compared with Case Studies 1 and 2. Under this most demanding condition, ABSMC exhibits a pronounced degradation in tracking accuracy, with the RMSE increasing to 32.27×10^{-5}, approximately 6.3 times higher than that of PI-SMC and about 2-3 times larger than its own RMSE values observed in the previous cases. This behavior indicates that sustained oscillations under pure CPL lead to considerable accumulated regulation error over the evaluation interval. By contrast, the proposed LESO-BSMC maintains the best overall performance, achieving the lowest RMSE $\left(1.473 \times 10^{-5}\right)$ and IAE $\left(8.631 \times 10^{-9}\right)$, corresponding to about 71% and 95% RMSE reduction relative to PI-SMC and ABSMC, respectively. The associated control-effort indices further reinforce this distinction: TVu decreases to 1.505×10^{3} and RMS(Δu) to 0.06934 , representing roughly a 90% reduction in total control variation compared with PI-SMC and nearly a tenfold decrease in RMS(Δu). Notably, the control effort remains consistently lower than that observed in the previous case studies.

Overall, these quantitative results confirm that LESO-based disturbance reconstruction enhances both regulation accuracy and switching-activity suppression under severe nonlinear CPL dynamics, whereas ABSMC tends to trade reduced control effort for substantially larger accumulated tracking error when parallel damping is absent.

3.4. Case Study 4: Simultaneous Input Voltage and CPL Variation

The last case study considers the most comprehensive disturbances scenario, in which both the input voltage and the constant-power load vary according to the profiles in Figs. 4 and 5, respectively, while a 15Ω resistor is connected in parallel with the CPL. The corresponding DC-bus voltage responses of the three controllers are depicted in Fig. 7, and the tracking and control effort indices are summarized in Table 5. In this scenario, the DC bus is subjected to concurrent source and load perturbations, whereas all controllers attempt to maintain 24 V .

At t $=$ 1.6 s, the input voltage drops from 18 V to 13 V while the CPL simultaneously decreases from 60 W to 0 W , producing a significant mixed disturbance on the DC bus. Among the three controllers, the ABSMC exhibits the

Table 4. Tracking and Control Effort Indices in Case Study 3

	RMSE	IAE	TVu	RMS($\Delta\mathbf{u}$)
PI-SMC	5.113×10^{-5}	3.144×10^{-8}	1.527×10^{4}	0.6663
ABSMC	32.27×10^{-5}	2.688×10^{-7}	1.254×10^{4}	0.6200
LESO-BSMC	1.473×10^{-5}	8.631×10^{-9}	1.505×10^{3}	0.06934

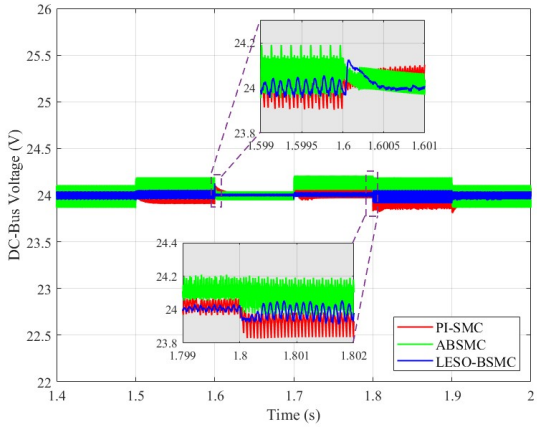

Fig. 7. DC-Bus Voltage Responses.

largest ripple amplitude of approximately 0.1 V together with pronounced high-frequency, indicating that its sliding dynamics remain highly sensitive to the combined input-voltage dip and load removal. The PI-SMC exhibits a small overshoot reaching approximately 24.11 V , followed by a gradual decay of oscillations. The voltage settles within roughly $8 - 10$ ms, with a residual ripple band of about ± 0.04 V around the 24 V reference. On the other hand, the proposed LESO-BSMC exhibits only a negligible overshoot over a very short interval and rapidly confines the voltage deviation to a very narrow band around 24 V while suppressing the oscillations much faster, demonstrating strong robustness to simultaneous source-load disturbances.

At $t = 1.8$ s, the CPL undergoes a sharp increase from 20 W to 80 W while the input voltage concurrently rises from 19 V to 20 V , creating a heavy-load disturbance on the DC bus. The PI-SMC shows a pronounced undershoot to about 23.83 V with increased oscillation amplitude and a longer settling process than during the disturbance at t $= 1.6$ s, reflecting reduced damping under the compounded perturbation. The ABSMC generates a smaller deviation than PI-SMC but exhibits the largest ripple, exceeding 0.2 V , together with a prolonged oscillatory behavior. Notably, the proposed LESO-BSMC maintains only a slight deviation around 24 V , attenuates the transient rapidly, and preserves a moderate ripple level of roughly 0.15 V , thereby achieving the most favorable overall performance among the three controllers.

The quantitative results summarized in Table 5 further confirm the consistent trends observed across the previous case studies. In terms of tracking accuracy, PI-SMC yields lower error indices than ABSMC, whereas ABSMC achieves smoother control action with lower TVu and reduced RMS(Δu). This behavior is consistent with the adaptive switching-gain mechanism of ABSMC [22], which mitigates conservative gain selection and reduces highfrequency oscillations. In contrast, the proposed LESO-BSMC consistently achieves the lowest RMSE and IAE among the three controllers while effectively suppressing chattering. This improvement is quantitatively supported by the smallest TVu and RMS(Δu) values among the compared strategies. By reconstructing structured disturbances in real time through the dualchannel LESO, uncertainties are compensated systematically rather than through increased switching gains, resulting in reduced high-frequency oscillations while maintaining global stability. These results demonstrate a superior balance between tracking accuracy and switching activity under CPL and input voltage variations.

Across all four case studies, the proposed LESO-BSMC strategy consistently exhibits superior regulation robustness and reduced switching activity under diverse source and load disturbances, providing comprehensive quantitative validation of its effectiveness for DC-bus voltage control in DC microgrids.

4. Conclusions

This paper has presented an integrated control strategy that combines a LESO with a BSMC for DC-bus voltage regulation in DCMGs. The obtained results of four comprehensive case studies demonstrate that the proposed controller consistently outperforms in comparison to PI-SMC and ABSMC strategies. The LESO-BSMC maintains the reference DC-bus voltage at 24 V and achieves the lowest RMSE, and IAE values, while providing faster recovery and significantly reduced voltage ripple. Furthermore, the proposed controller exhibits the smallest control-effort indices (TVu and RMS(Δu)), confirming effective chattering mitigation and reduced switching activity under diverse disturbance scenarios. These findings verify that the em-

Table 5. Tracking and Control Effort Indices in Case Study 4

	RMSE	IAE	TVu	RMS(Δu)
PI-SMC	6.008×10^{-5}	4.039×10^{-8}	1.548×10^{4}	0.6640
ABSMC	13.64×10^{-5}	9.736×10^{-8}	1.054×10^{4}	0.5716
LESO-BSMC	3.289×10^{-5}	2.126×10^{-8}	2.907×10^{3}	0.1243

bedded LESO accurately reconstructs lumped disturbances, thereby enhancing the robustness and regulation accuracy of the sliding-mode framework under severe operating conditions.

Based on these results, the proposed LESO-BSMC strategy shows strong potential for practical implementation in various DC-DC converter configurations. Although residual chattering cannot be completely eliminated due to the inherent nature of SMC, the demonstrated reduction in switching activity further supports its practical real-time applicability. Importantly, the proposed controller consists only of low-order observer dynamics and explicit algebraic control laws, without requiring online optimization, matrix inversion, or high-dimensional computations. This results in moderate computational complexity, making the strategy suitable for implementation on DSP-based or embedded realtime platforms operating at typical switching frequencies.

Future work will focus on experimental validation through real-time DSP implementation and hardware-in-the-loop (HIL) testing. Further research will also investigate bandwidthadaptive LESO mechanisms and gain-tuning strategies for the SMC layer, as well as extension to coordinated or hierarchical DCMG architectures to evaluate scalability and multi-converter operation.

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Appendix a

Stability Analysis of the Dual-Channel LESO Estimation Errors

Using Eq. (9) - Eq. (13), the error dynamics of each channel can be written compactly as:

$$\dot{e}_i = A_{oi} e_i + \begin{bmatrix} 0 \\ \dot{h}_i \end{bmatrix}, \quad A_{oi} = \begin{bmatrix} -L_{i1} & 1 \\ -L_{i2} & 0 \end{bmatrix} \tag{A1}$$

Substituting the chosen gains from Eq. (11) yields:

$$A_{oi} = \begin{bmatrix} -2\omega_{0i} & 1 \\ -2\omega_{0i}^2 & 0 \end{bmatrix} \tag{A2}$$

The characteristic polynomial of A_{oi} becomes:

$$s^2 + 2\omega_{0i} s + \omega_{0i}^2 = (s + \omega_{0i})^2 \tag{A3}$$

which has a repeated root at $s = -\omega_{0i} < 0$. This ensures that the homogeneous error dynamics are exponentially stable. Consequently, for constant disturbances, both e_{i1} and e_{i2} converge to zero exponentially.

For time-varying disturbances satisfying Assumption 2, the term $\dot{h}_i$ acts as an external excitation. Since A_{oi} is Hurwitz for any $\omega_{0i} > 0$, the error dynamics are input-to-state stable. Additionally, the steady-state estimation error can be made arbitrarily small by increasing the observer bandwidth ω_{0i}. This property guarantees robust disturbance reconstruction, which is essential for the subsequent backstepping sliding mode control design.

Appendix b

Lyapunov-Based Stability Proof of the LESO-Compensated Control Law

The derivative of Lyapunov can be expressed by substituting Eq. (27) into Eq. (28) as follows:

$$\dot{V}_2 = -K_1 e_1^2 + e_1 e_2 + e_1 \tilde{h}_1 - K_2 \sigma^2 - K_S |\sigma| \tag{B1}$$

$$\text{where:} \quad e_2 = \sigma - \lambda_1 e_1 - \lambda_2 \int_0^t e_1(\tau) d\tau \tag{B2}$$

And Young's inequality, there exists $\varepsilon \in (0, 2K_2)$ such that:

$$\dot{V}_2 \leq -\left(K_1 + \lambda_1 - \frac{1}{2\varepsilon}\right) e_1^2 - \left(K_2 - \frac{\varepsilon}{2}\right) \sigma^2 - K_S |\sigma| + e_1 \tilde{h}_1 \tag{B3}$$

Under the LESO design in Section 2.4, the disturbance estimation error $\tilde{h}_1$ can be made arbitrarily small by increasing the observer bandwidth and remains bounded for all operating conditions. As a result, the closed-loop system is globally asymptotically stable when $\tilde{h}_1 \to 0$, and practically stable (ISS with respect to $\tilde{h}_1$) when $\tilde{h}_1$ is bounded. This guarantees robust voltage regulation and effective disturbance rejection even under rapid variations of the input voltage and CPL demand.

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