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Voltage- and Current-Modes Sinusoidal Oscillator Using a Single Differential Voltage Current Conveyor

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Abstract

This paper presents a new sinusoidal oscillator using a single differential voltage current conveyor (DVCC) and five passive components. The proposed oscillator concurrently provides voltage output and current output, and can independently control the oscillation condition without affecting oscillation frequency. The proposed circuit has a dual-mode (i.e., voltage and current modes) operation property, including low active and passive sensitivities, as well as a desirable total harmonic distortion (THD). This study first introduces the DVCC device and the proposed oscillator circuit, and thereafter presents the non-ideal effects and the results of the sensitivity study of the proposed circuit. This study conducted simulations for the proposed circuit using HSPICE, and used commercial ICs and discrete components for circuit implementation and testing to verify its feasibility. Computer simulations and experimental results confirmed the validity of theoretical analysis.

***Key Words*:** Active RC Circuit Design, Current-Mode Circuit, Differential Voltage Current Conveyor, Sinusoidal Oscillator

1. Introduction

A sinusoidal oscillator is an important basic component, which has numerous applications in communication modules, instrumentation and measurement equipment, power conversion control circuits, power amplifier controller designs, and medical circuit systems. In early active RC circuit designs, sinusoidal oscillators were easily constructed by combining operational amplifiers (OPAs) with a few external passive components; these established circuit topologies have been widely used for a long time [1]. Since the concept of current-mode analog circuit signal-processing technology was introduced, it has become an important circuit design type for analog circuit designers because of its high performance, versatile function, and simple implementation [2]. In 1968, Smith and Sedra introduced the first current-mode active device — the current conveyor [3]. Since that point, many active devices have been developed and have been used for various applications [4–9]. In addition to the conventional method of using OPAs to construct sinusoidal oscillators, previous studies have proposed several implementations for sinusoidal oscillators using various types of active devices [10–15]. In 1989, Pal first introduced the differential voltage current conveyor (DVCC) device and reported the construction of a few DVCC-based application circuits [16]. This device in CMOS implementation has been developed and realized next by Elwan and Soliman [17]. Subsequently, several newest CMOS circuit implementations of DVCC were reported in [18–20]. To date, DVCC devices have been used in numerous electronic circuit designs, such as active filters, quadrature oscillators, monostable multivibrators, pulse width modulator, and square/triangular waveform generators [21–24]. In addition, previous studies have presented several implementations for sinu-

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soidal oscillators using DVCC [25–28]. A circuit topology operated in voltage-mode was created using a single DVCC combined with two resistors and two capacitors [26]. This circuit was the first reported voltage-mode sinusoidal oscillator using DVCC. Another study presented a current-mode design that used a single DVCC and five additional passive components [25]; however, only three passive components were grounded for the circuit. This circuit represented the first study on using a DVCC to realize a current-mode sinusoidal oscillator. Another study revealed an improved topology that reduced the number of passive components [27]. This circuit was composed of a DVCC combined with two floating resistors and two grounded capacitors, and is a simpler circuit topology compared to existing topologies that operate in current-mode. In 2007, Kumar, Keskin, and Pal proposed DVCC-based dual-mode sinusoidal oscillators [28]. Each circuit was constructed using two DVCCs and five passive components. To the best of our knowledge, this was the first dual-mode sinusoidal oscillator to use DVCC. However, these circuits require a greater number of active devices. Although DVCC-based sinusoidal oscillators have been discussed in previous studies, existing topologies use complementary current output terminals (Z+ and Z- terminals) for the DVCC (Except for one that uses voltage-mode [26]). These oscillators require a more complex internal circuit realization for the DVCC (i.e., they require excessive numbers of transistors to perform the function of the Z- terminal). No study has attempted to use single DVCC to construct dual-mode sinusoidal oscillators. This study presents a feasible scheme to satisfy this need. The proposed circuit uses a DVCC and five passive components, and can simultaneously operate under voltage and current modes. The rest of this paper is arranged as follows: section 2 introduces the active device DVCC and presents the proposed sinusoidal oscillator and the related governing equations. Section 3 introduces the non-idealities issues and the sensitivity study on the proposed circuit. Section 4 provides a viable design procedure for the oscillation condition and the oscillation frequency for the proposed oscillator, thereafter demonstrating the effectiveness of the circuit by presenting simulation and experimental results. Finally, section 5 offers a conclusion.

2. The Proposed Voltage and Current Modes Sinusoidal Oscillator

The DVCC is currently a popular active device in analog circuit designs because it can operate in both differential and non-differential signal-processing modes. Therefore, a DVCC device provides flexibility and enables various circuit implementations [21–28]. The circuit symbol for a DVCC used in this paper is shown in Figure 1, and includes two high-impedance voltage input terminals (Y_1 and Y_2), one low-impedance current output terminal (X), and two high-impedance current output terminals (Z+). The terminal relationships of an ideal DVCC are defined in (1), where the X terminal voltage follows the voltage difference of terminals Y_1 and Y_2, the current flow into the Y_1 and Y_2 terminals is zero, and the current flow out of terminal X is conveyed to terminal Z+ with the same flow direction. An ideal DVCC exhibits zero input impedance at terminal X and infinite resistances at both Y terminals, as well as at the Z+ terminals.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{1}$$

Although previous studies have presented several implementations of CMOS DVCC [17–20], a compact CMOS DVCC is shown in Figure 2, which was obtained by modifying the circuit presented in [29]. This circuit

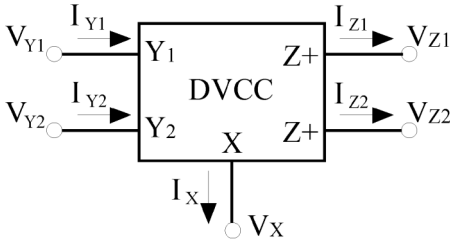

Figure 1. Circuit symbol of a DVCC.

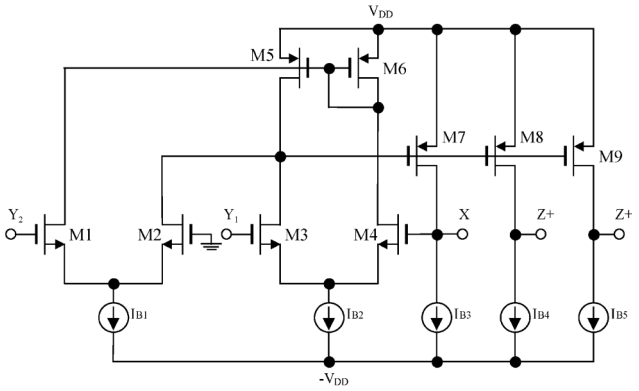

Figure 2. A compact CMOS implementation of the DVCC.

was composed of a voltage difference circuit (M_1–M_7) and a current duplicate circuit (M_8–M_9) to perform the functions of the X terminal voltage follows the voltage difference of input terminals Y_1 and Y_2, and the current that flowed out of terminal X was replicated to the Z+ terminals, respectively. In this circuit, the substrate terminals of all PMOS and NMOS transistors are connected to positive and negative supply voltages, respectively. It makes the operation of the circuit insensitive to the threshold voltage variation caused by the body effects.

A DVCC can also be implemented using commercially available ICs. Figure 3 shows a DVCC device constructed with AD844AN ICs [23]. The AD844AN ICs had the following properties: the inverting and non-inverting input terminals exhibited an inherent virtual short property, and the current into the inverting terminal was replicated to terminal T_z [30]. In this manner, the non-inverting input terminals of the first and second AD844ANs were used to simulate the two high-impedance inputs (Y_1 and Y_2) of a DVCC, as shown in Figure 1. To produce a terminal voltage V_X proportional to the difference of the Y_1 and Y_2 voltages, the resistor R_a was placed between the inverting input terminals of the first and second AD844ANs, and then the grounded resistor R_b was used to connect the T_z terminal of the first AD844AN and the non-inverting input terminal of the third AD844AN. The fourth and fifth AD844ANs and resistors R_c, R_d, and R_e performed the function of output currents I_{Z1} and I_{Z2}, respectively. The resulting expressions of the related currents are included in Figure 3. Referring to Figure 3, the relationships among these voltages and currents were determined using (2).

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & R_b/R_a & -R_b/R_a & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_c/R_d & 0 & 0 & 0 \\ R_c/R_e & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \quad (2)$$

Therefore, if the conditions $R_a = R_b$ and $R_c = R_d = R_e$ are settled, the terminal behavior of the applied DVCC (Figure 3) is nearly ideal. Because the AD844AN IC is widely used to implement various electronic circuits, the realization shown in Figure 3 provides a viable manner to implement a DVCC, which is currently commercially unavailable. Figure 4 shows the circuit diagram of the proposed sinusoidal oscillator, which is composed of a single DVCC and five passive components (only one had a float-

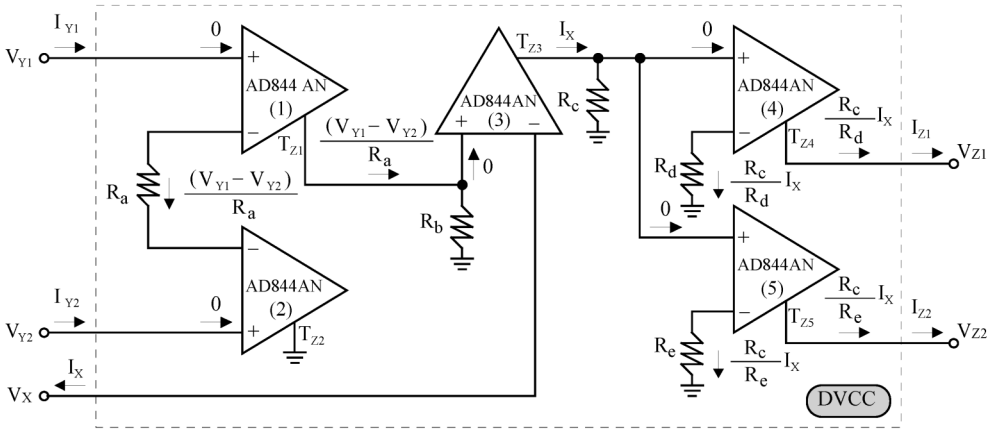

Figure 3. DVCC constructed using commercially available ICs.

ing connection). Assuming an ideal DVCC characterized by (1) and executing a routine circuit analysis yielded the characteristic equation of the circuit expressed in (3), the oscillation condition and oscillation frequency of the circuit were determined in (4) and (5), respectively.

$$S^2R_1R_2C_1C_2 + S(R_1C_2 + R_2C_1 + R_1C_1 - \frac{R_1R_2}{2R_3}C_1) + 1 = 0 \tag{3}$$

$$R_3 = \frac{R_2}{2\left(1+\frac{R_2}{R_1}+\frac{C_2}{C_1}\right)} \tag{4}$$

$$\omega_o = 2\pi f_o = \sqrt{\frac{1}{R_1R_2C_1C_2}} \tag{5}$$

Equations (4) and (5) show that the oscillation condition is independently controlled by the resistor R_3 without affecting the oscillation frequency. Section 4 presents a feasible design procedure of the oscillation condition and oscillation frequency for the presented circuit. Compared to the circuits reported in [28], the proposed topology uses fewer active devices to realize a dual-mode sinusoidal oscillator. Another feature is that the DVCC device that appeared in the circuit (Figure 4) only requires current output terminals (Z+) rather than uses complementary current output terminals (Z+ and Z- terminals). Thus, for the proposed circuit, the internal circuit of a CMOS DVCC is simpler than the previous designs [25] and [27,28], which adopts the DVCC with both the Z+ and Z- terminals. Because of the proposed dual-mode operation featured in the sinusoidal oscillator in conjunction with its simplicity, this circuit could be expected to find wide applications in communication, instrumentation, measurement, control, and power systems.

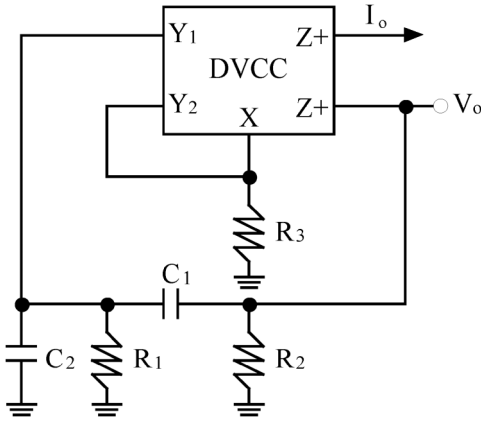

Figure 4. DVCC-based voltage and current modes sinusoidal oscillator.

3. Effect of Non-Idealities and Sensitivity Study

This section presents several non-ideal issues to determine the influences of non-ideal effects on the proposed circuit (Figure 4). A practical DVCC can be considered an ideal DVCC with finite parasitic resistances and non-ideal voltage and current transfer gains. Figure 5 shows the non-ideal circuit model of a DVCC with parasitic resistances. In Figure 5, terminal X' exhibits a low-value parasitic series resistance R_x (in the range of several ohms), whereas terminals Y_1', Y_2', and Z+' reveal high-value parasitic parallel impedances R_y and R_z, respectively (in the range of a few mega-ohms). By examining the effects of the parasitic resistances (R_x, R_y, and R_z), as well as the non-ideal voltage and current transfer gains, the terminal relationships of the non-ideal DVCC (Figure 5) can be determined in (6).

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} -R_x & \alpha & -\alpha & 0 & 0 \\ 0 & 1/R_y & 0 & 0 & 0 \\ 0 & 0 & 1/R_y & 0 & 0 \\ \beta & 0 & 0 & -1/R_z & 0 \\ \beta & 0 & 0 & 0 & -1/R_z \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{6}$$

In (6), α denotes the non-ideal voltage transfer gain

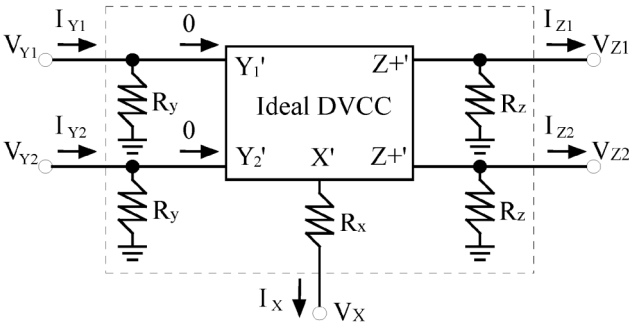

Figure 5. Non-ideal circuit model of the DVCC.

from the Y' terminals to the X' terminal of the DVCC, and β represents the non-ideal current transfer gain from the X' terminal to the Z+' terminal of the DVCC. The standard values of the non-ideal voltage and current transfer gains ranged from approximately 0.8 to 0.9 and had an ideal value of 1. Following the application of the non-ideal circuit characteristic expressed in (6) to the proposed circuit (Figure 4), tedious analyses led to the modified characteristic equation expressed in (7). The modified oscillation condition was determined in (8), whereas the oscillation frequency had the same formula expressed in (5).

$$S^2R_1R_2C_1C_2 + S(R_1C_1 + R_2C_1 - \frac{\alpha\beta R_1R_2}{(1+\alpha)R_3}C_1 + R_1C_2) + 1 = 0 \quad (7)$$

$$R_3 = \frac{\alpha\beta R_2}{(1+\alpha)\left(1+\frac{R_2}{R_1}+\frac{C_2}{C_1}\right)} \quad (8)$$

In (7) and (8), the following conditions were applied: $R_z >> R_2$, $R_y >> R_1$, $R_y >> R_3$, $R_1 >> R_x$, $R_z >> 1$, and $R_y >> 1$. To negate these parasitic effects on the proposed circuit (Figure 4), suitable values of R_1, R_2, and R_3 ranged from several hundred ohms to several tens of kilo ohms. Equation (8) shows that the non-ideal voltage and the current transfer gains influenced the oscillation condition. However, this problem was overcome by slightly retuning the value of R_3 to start the oscillation process. Using (5), the active and passive sensitivities of the proposed circuit were derived by (9).

$$S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2}$$
$$S_{R_x}^{\omega_o} = S_{R_y}^{\omega_o} = S_{R_z}^{\omega_o} = S_{\alpha}^{\omega_o} = S_{\beta}^{\omega_o} = 0 \quad (9)$$

Equation (9) shows that all active and passive sensitivities were lower than the unity in magnitude. Therefore, $R_z >> R_2$, $R_y >> R_1$, $R_y >> R_3$, $R_1 >> R_x$, $R_z >> 1$, and $R_y >> 1$ conditions must be satisfied in the design procedures to minimize the influence of the non-ideal effects and sensitivities factors on the proposed circuit.

4. Design Procedures and Experimental Results

This study presents a number of simulation and experimental examples to demonstrate the validity of the theoretical analysis. The proposed circuit (Figure 4) was simulated with HSPICE computer simulation using the implementation of CMOS DVCC shown in Figure 2. The transistor model parameters were taken from a TSMC 0.35 μm CMOS parameter process with supply voltages V_{DD} = $-V_{DD}$ = 2.5 V and bias currents $I_{B1} = I_{B2} = I_{B3} = I_{B4} = I_{B5}$ = 50 μA. The aspect ratios of the MOS transistors were designed as follows: $(W/L)_{M1–M4}$ = 5.65/3.5, $(W/L)_{M5–M6}$ = 200/10, and $(W/L)_{M7–M9}$ = 22.5/2.2. Commercially available ICs (AD844ANs) and discrete passive components were used to construct the prototype circuit of the proposed circuit (Figure 4) to conduct experimental tests. All experiments were performed at supply voltages of ± 5 V with $R_a = R_b = R_c = R_d = R_e$ = 1 kΩ. A feasible design procedure of the oscillation condition and the oscillation frequency for the proposed oscillator was arranged as follows: first, $R_1 = R_2$ and $C_1 = C_2$ were assigned. Thereafter, the appropriate values for C_1 and C_2 were selected, and an oscillation frequency was specified. Therefore, the values of R_1 and R_2 can be determined using (5). Subsequently, R_3 was calculated using (4). To serve as an example, a circuit was designed with an oscillation frequency of f_o = 100 kHz with component values of $R_1 = R_2$ = 1.59 kΩ and $C_1 = C_2$ = 1 nF. In actuality, the value of R_3 was designed slightly smaller than the theoretical value (R_3 = 0.26 kΩ). It was necessary to change the value of R_3 = 0.21 kΩ to start the oscillations. This slight deviation was caused by the non-ideal voltage and current transfer gains, which were similar to those anticipated by (8). The simulation results of the time waveform for the output V_o are shown in Figure 6a. The oscillation frequency for the waveform shown in Figure 6a was measured as f_o = 96.15 kHz. Figure 6b shows the simulation results of the frequency spectrum for the output V_o. The percentage of the total harmonic distortion (THD%) was determined as 3.27%. Figure 7 shows the simulation results for the output I_o with time at a frequency of f_o = 96.15 kHz; its frequency spectrum exhibited a total harmonic distortion of 3.76%. In practice, the maximum and minimum amplitude swings

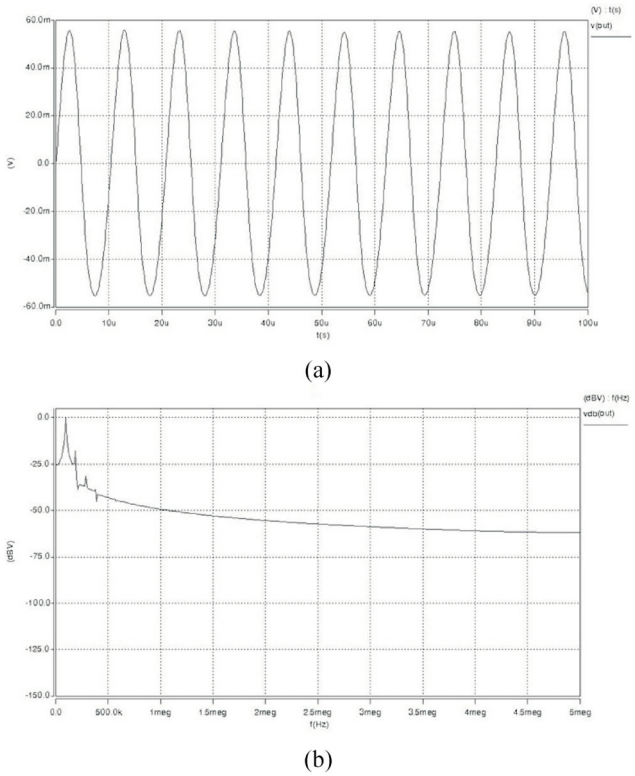

Figure 6. Simulation results of the voltage output V_o for the circuit (Figure 4): (a) output waveform in the steady state and (b) its frequency spectrum.

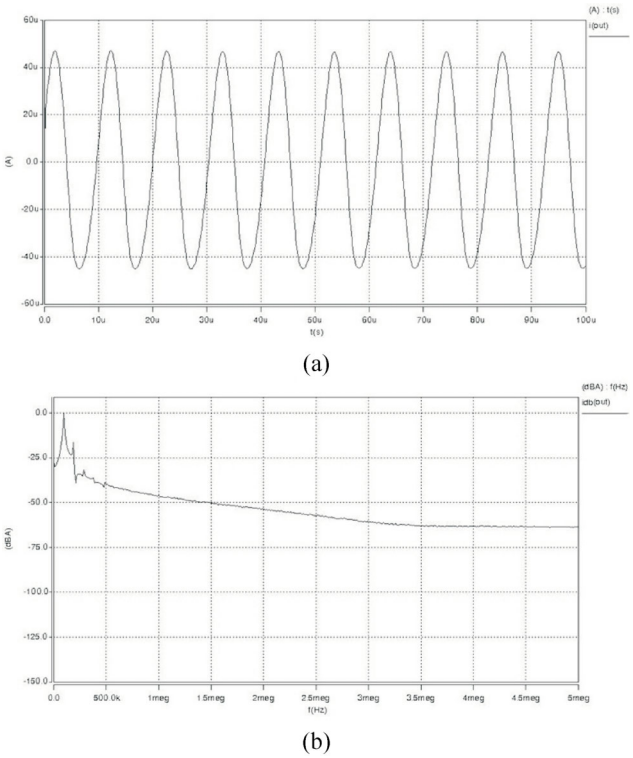

Figure 7. Simulation results of the current output I_o for the circuit (Figure 4): (a) output waveform in the steady state and (b) its frequency spectrum.

for the output waveforms are limited by the feasible operating supply voltages of the CMOS DVCC circuit (Figure 2). For the circuit (Figure 2), the feasible operating supply voltages range from $\pm V_{DD} = \pm 1.5$ V to ± 2.5 V. To attain the lowest and highest applicable operating frequency of the proposed circuit, a fastest way is to employ different capacitance values. By adopting $R_1 = R_2 = 1.59$ kΩ, $R_3 = 0.21$ kΩ, and $C_1 = C_2 = 0.13$ nF, Figure 8 shows the simulation results for the voltage and current output waveforms of the proposed circuit in the steady state with $f_o = 775.19$ kHz. The highest frequency of the proposed oscillator was only demonstrated at approximated several hundred of kHz. With regard to the lowest frequency opera-

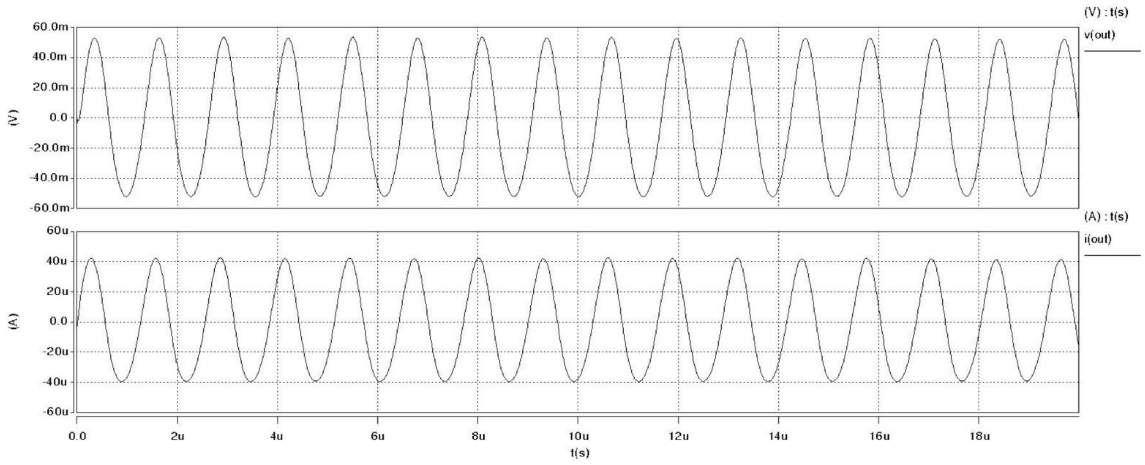

Figure 8. Simulation results of the highest applicable oscillations of the circuit (Figure 4).

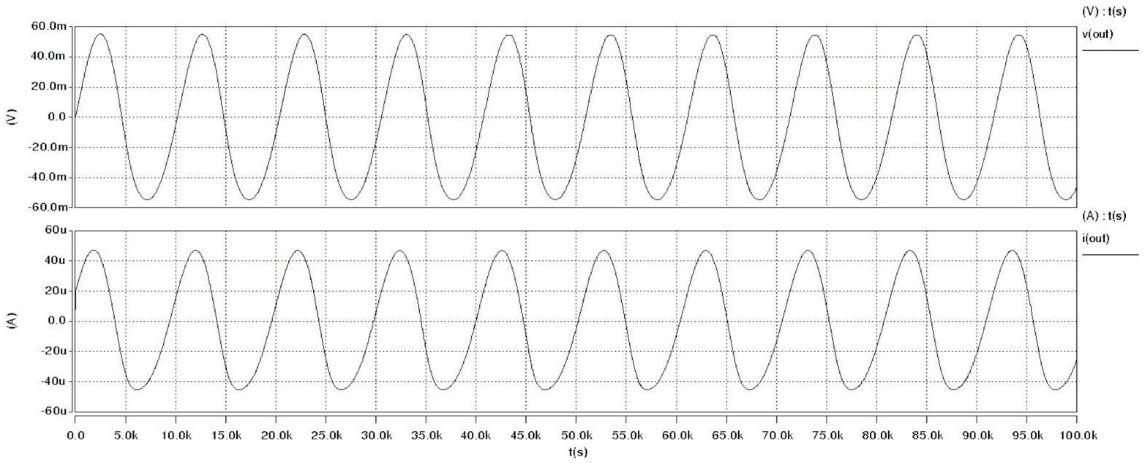

Figure 9. Simulation results of the lowest applicable oscillations of the circuit (Figure 4).

tion, an experimental test with values $R_1 = R_2 = 1.59$ kΩ, $R_3 = 0.21$ kΩ, and $C_1 = C_2 = 1$ F was executed to explore this characteristic. Figure 9 shows the test results for the lowest frequency of oscillation with $f_o = 0.1$ mHz. It was concluded that the oscillation frequency of the proposed sinusoidal oscillator (Figure 4) operated in a wide frequency range.

Regarding the experimental tests for the proposed circuit, the following component values were determined based on the design procedures $R_1 = R_2 = 1.59$ kΩ, $C_1 = C_2 = 1$ nF, and $R_3 = 0.23$ kΩ. As mentioned, R_3 was designed to be smaller than the theoretical value to ensure that oscillation occurred. The oscillations were built up in steady-state waveforms, and Figures 10a and 11a show the experimental results of the corresponding output waveforms for the voltage and current outputs, respectively. Experimental results showed an oscillation frequency of $f_o = 96.47$ kHz. The output frequency spectra of V_o and I_o are shown in Figures 10b and 11b, respectively. The total harmonic distortion for the voltage output was 3.33%, and the total harmonic distortion for the current output was 4.02%. These results verify that the experimental tests were in good agreement with the theoretical analyses, suggesting that the proposed oscillator can be implemented using commercially available ICs or CMOS technology.

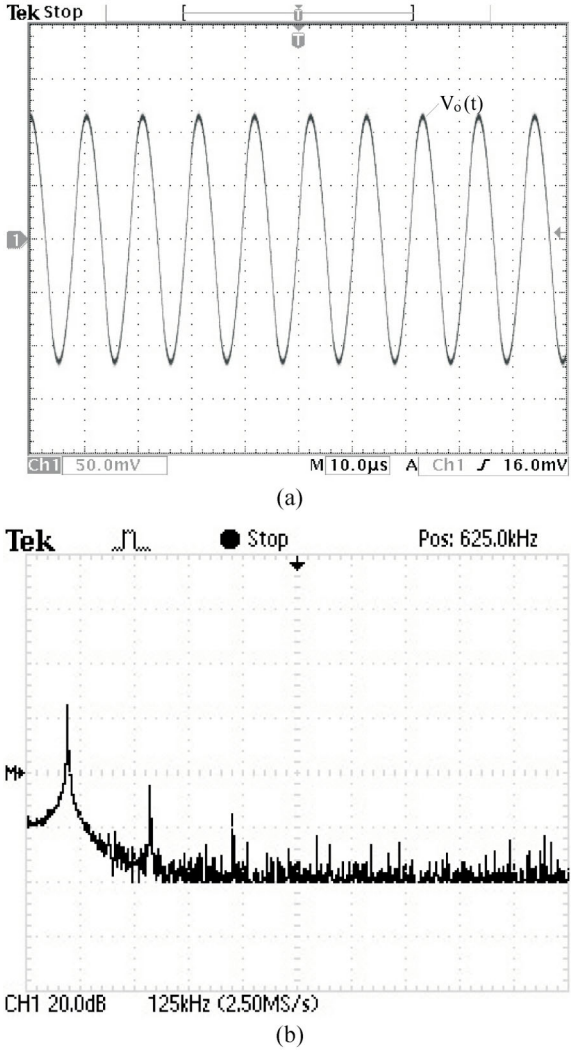

Figure 10. Experimental results of the corresponding output waveforms for the circuit (Figure 4): (a) Voltage output waveform and (b) Its frequency spectrum.

5. Conclusion

This study presented a novel voltage- and current-

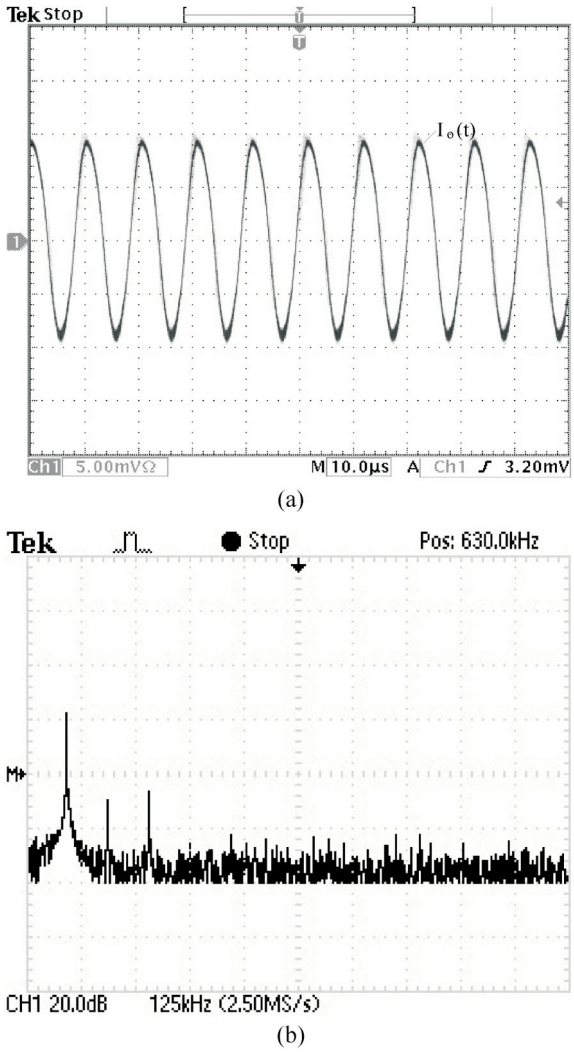

Figure 11. Experimental results of the corresponding output waveforms for the circuit (Figure 4): (a) Current output waveform and (b) Its frequency spectrum.

modes sinusoidal oscillator that was constructed using a single DVCC and five passive components. In addition, this study presented a description of the related governing equations of the proposed oscillator and the non-ideal effects on the circuit. HSPICE simulations with a TSMC 0.35 μm CMOS parameter process, as well as experimental tests applied to commercially available ICs, confirmed the feasibility of the proposed circuit. Because the proposed oscillator has a simple circuit topology and provides dual-modes of operation, this circuit could have a wide variety of applications in the future, such as in instrumentation, measurement, power, and communication systems.

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